

FIGURE 1

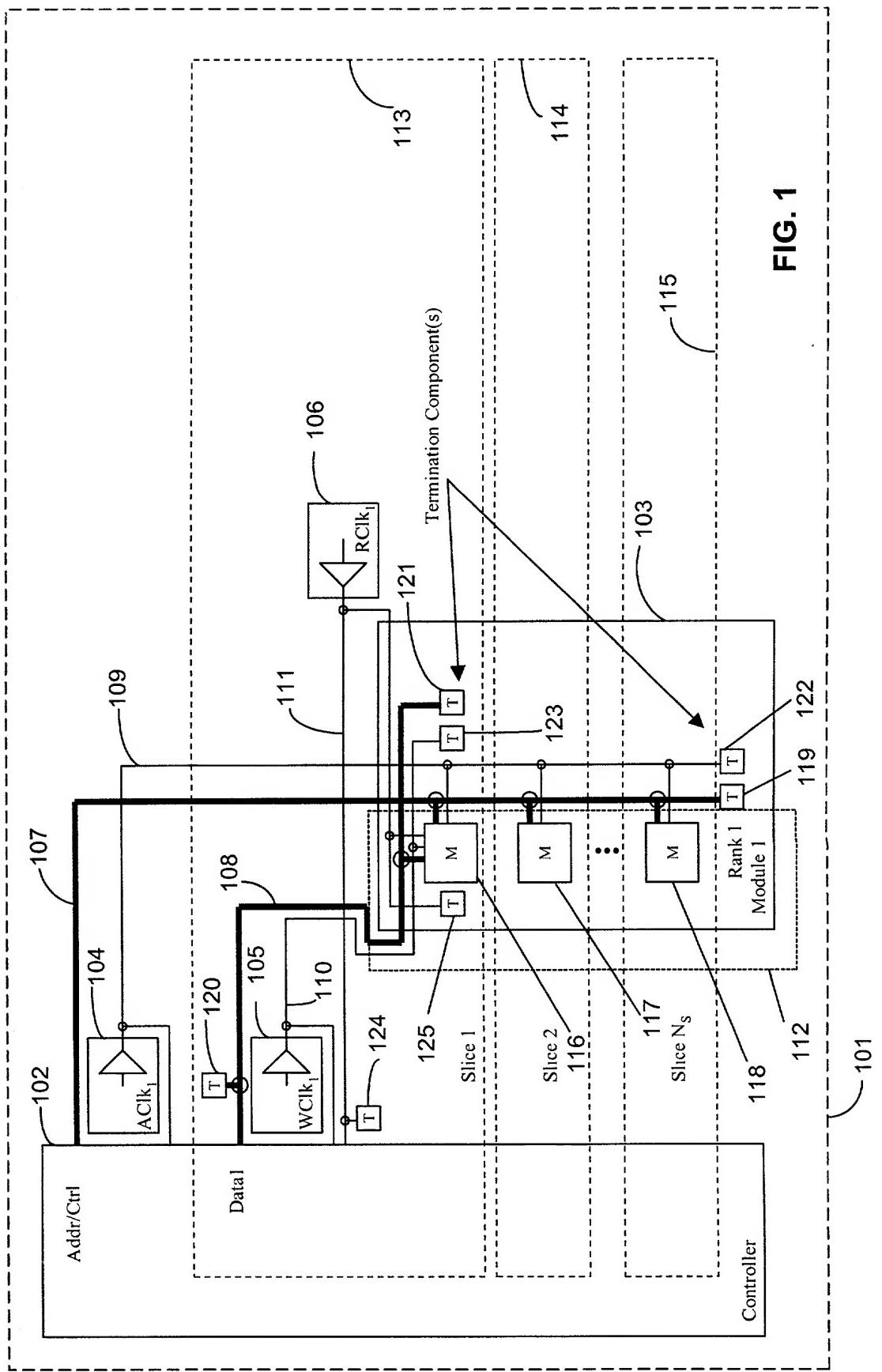
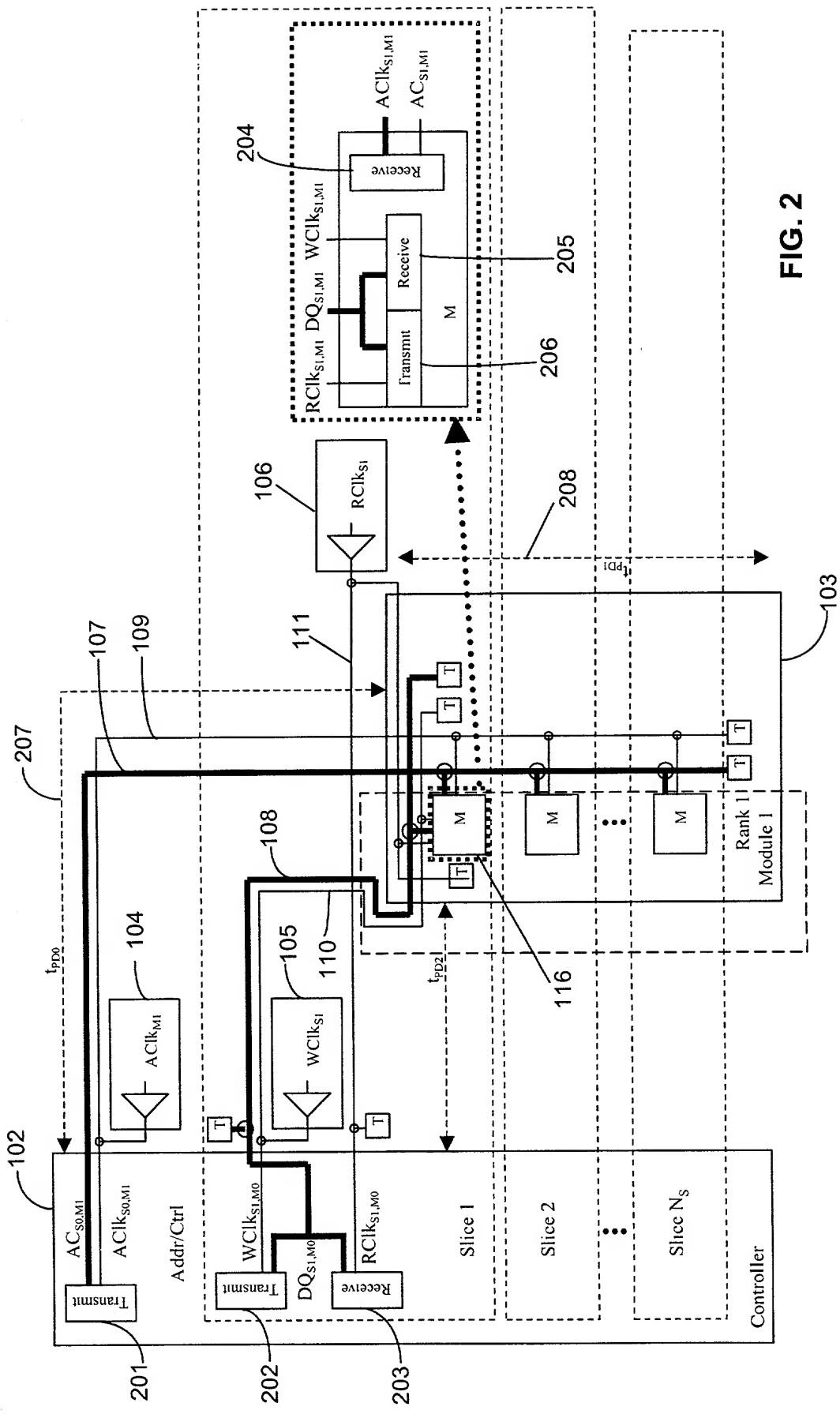


FIG. 1

FIG. 2



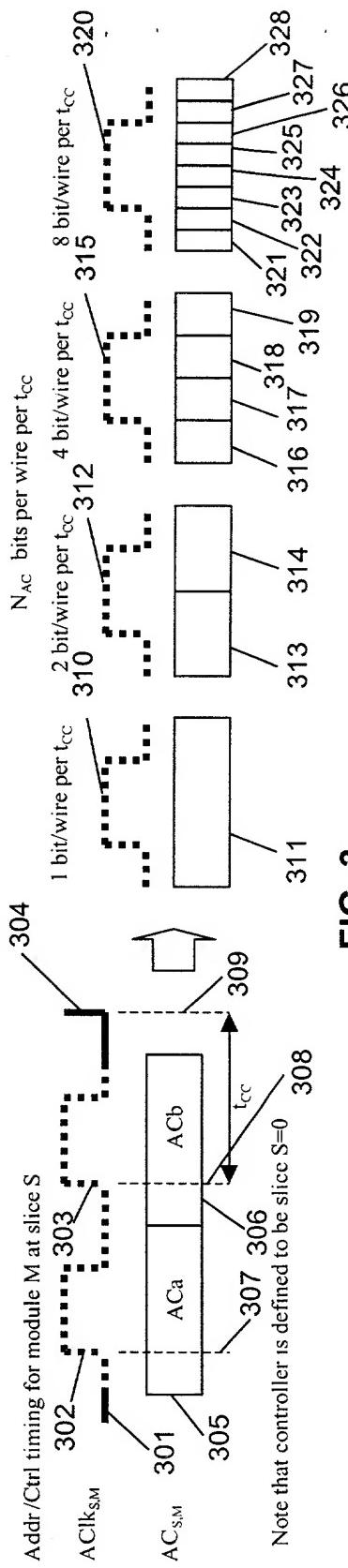


FIG. 3

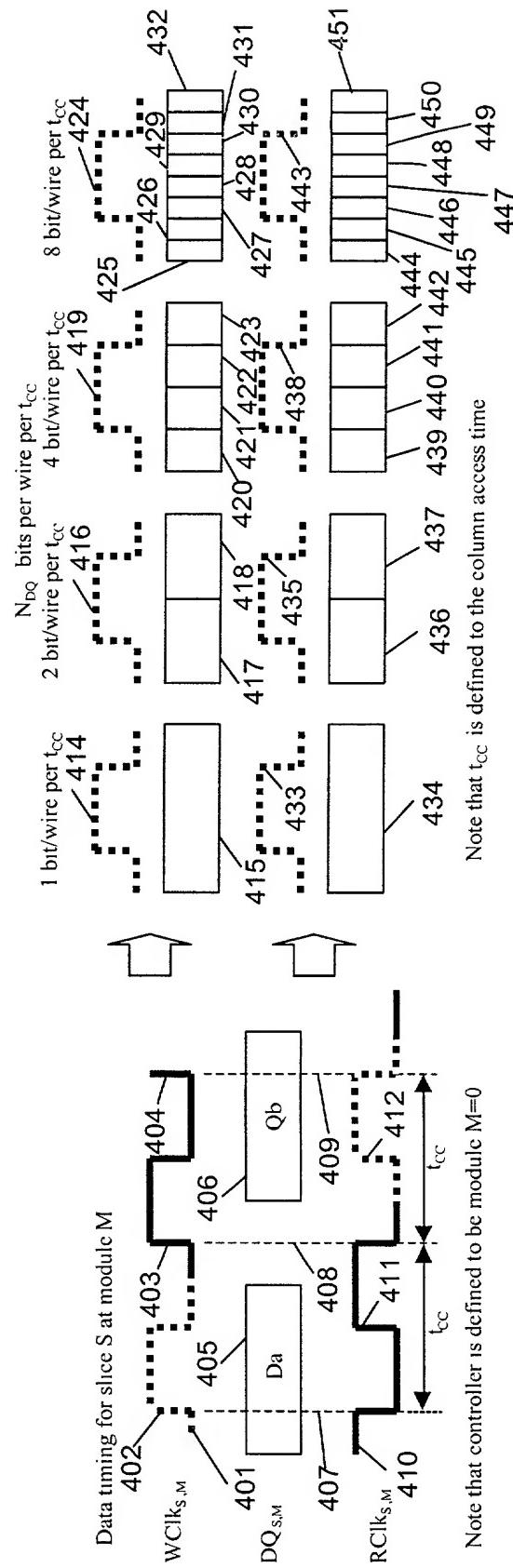


FIG. 4

FIG. 5

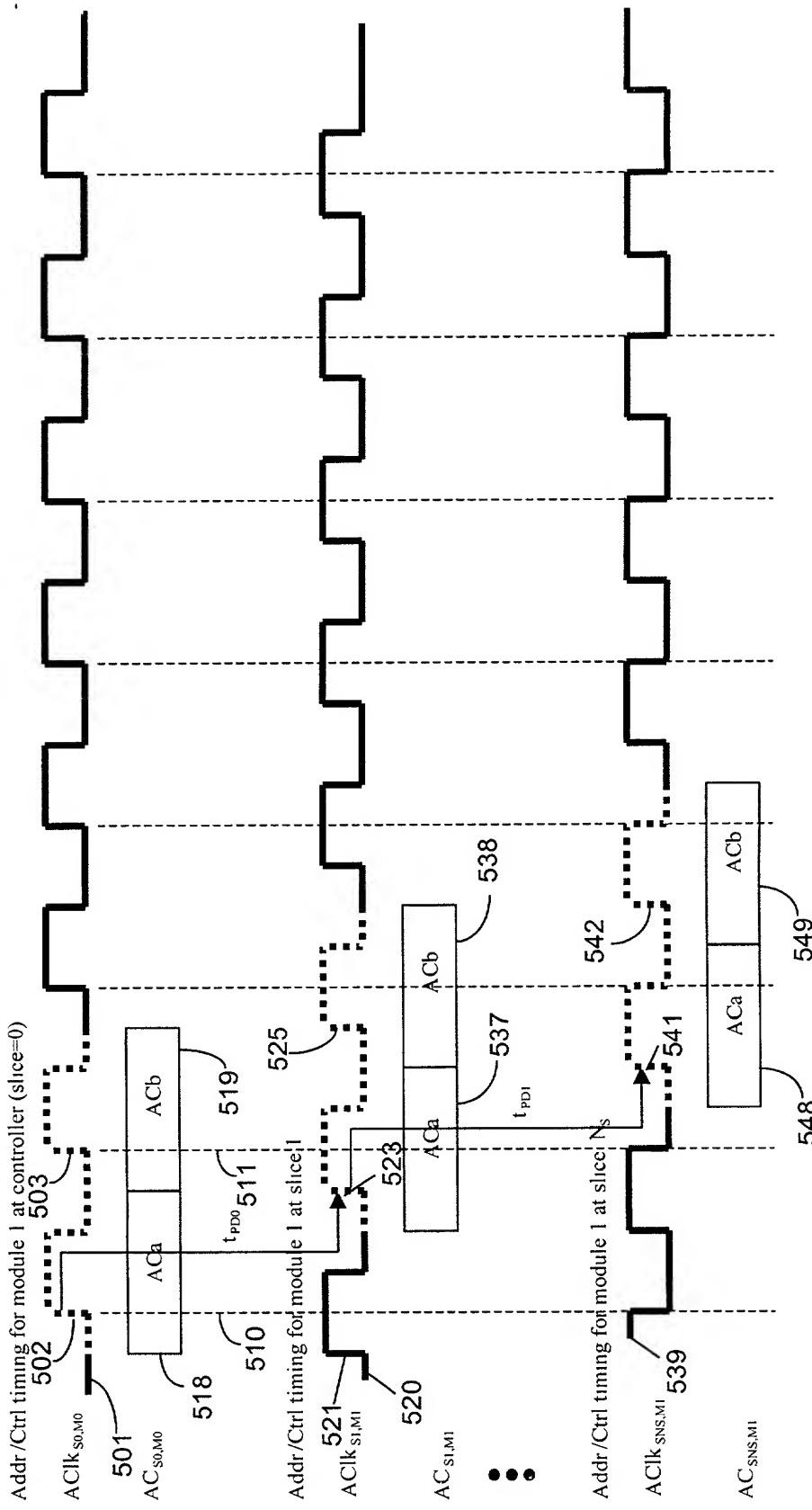


FIG. 6

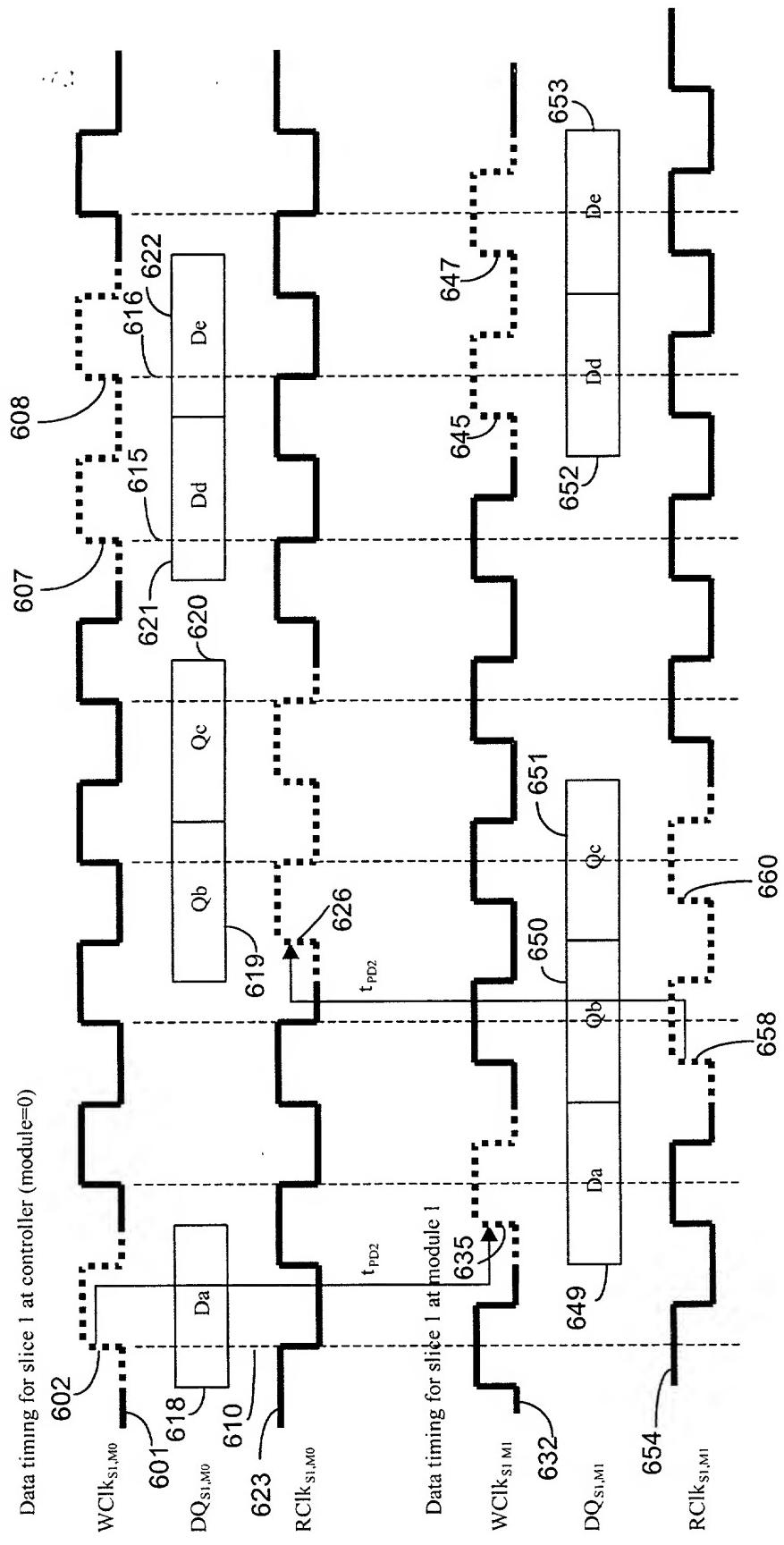


FIG. 7

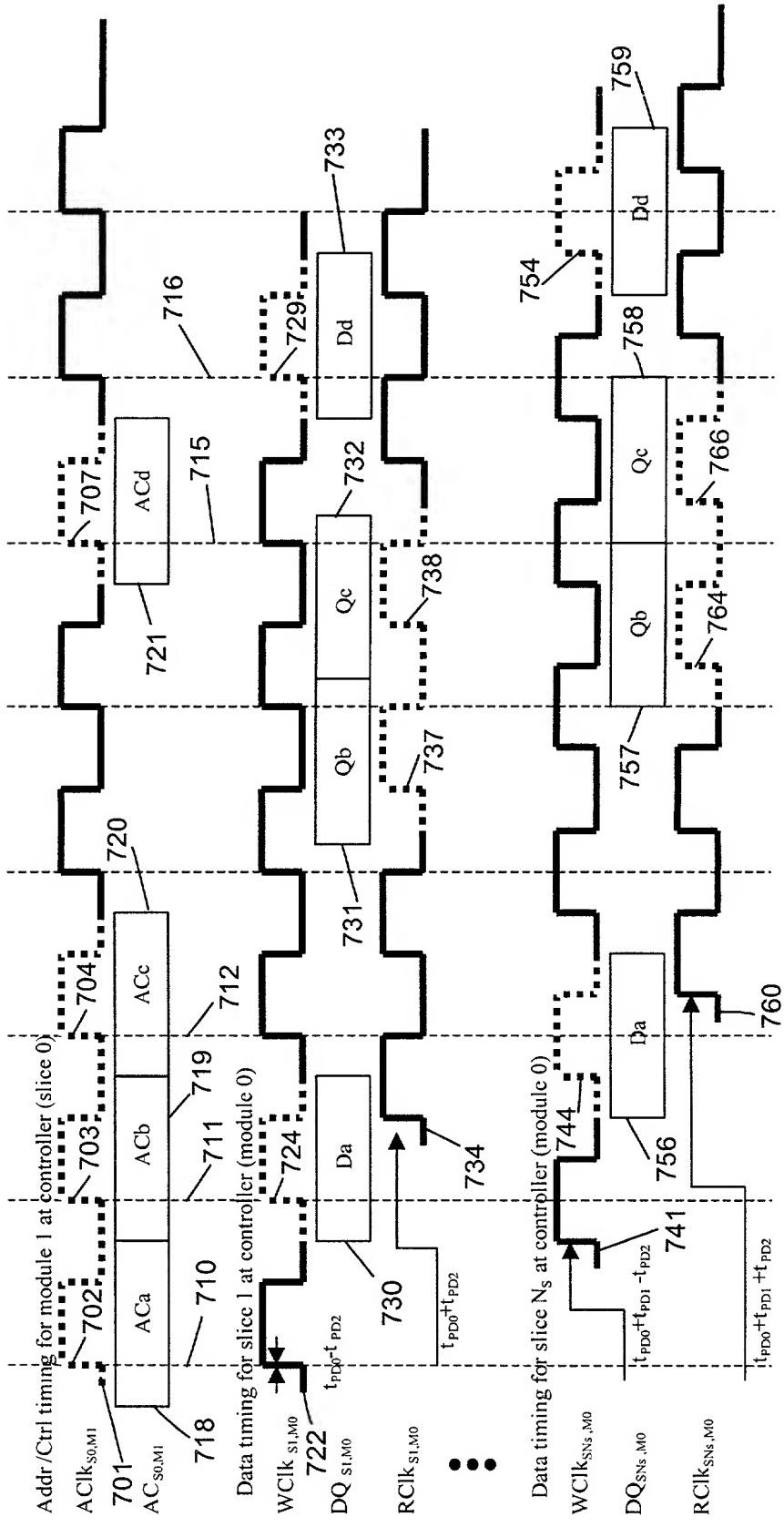


FIG. 8

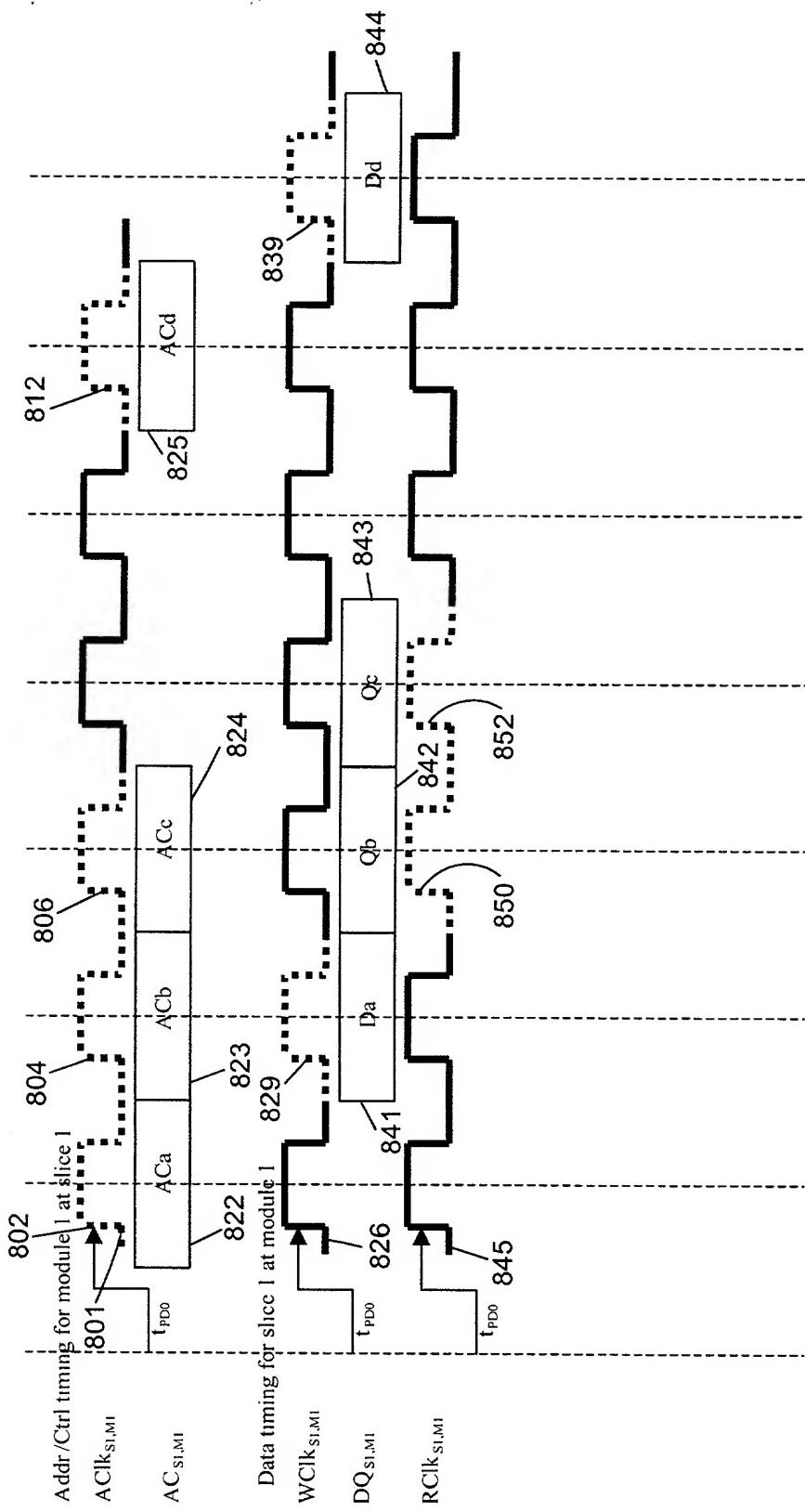


FIG. 9

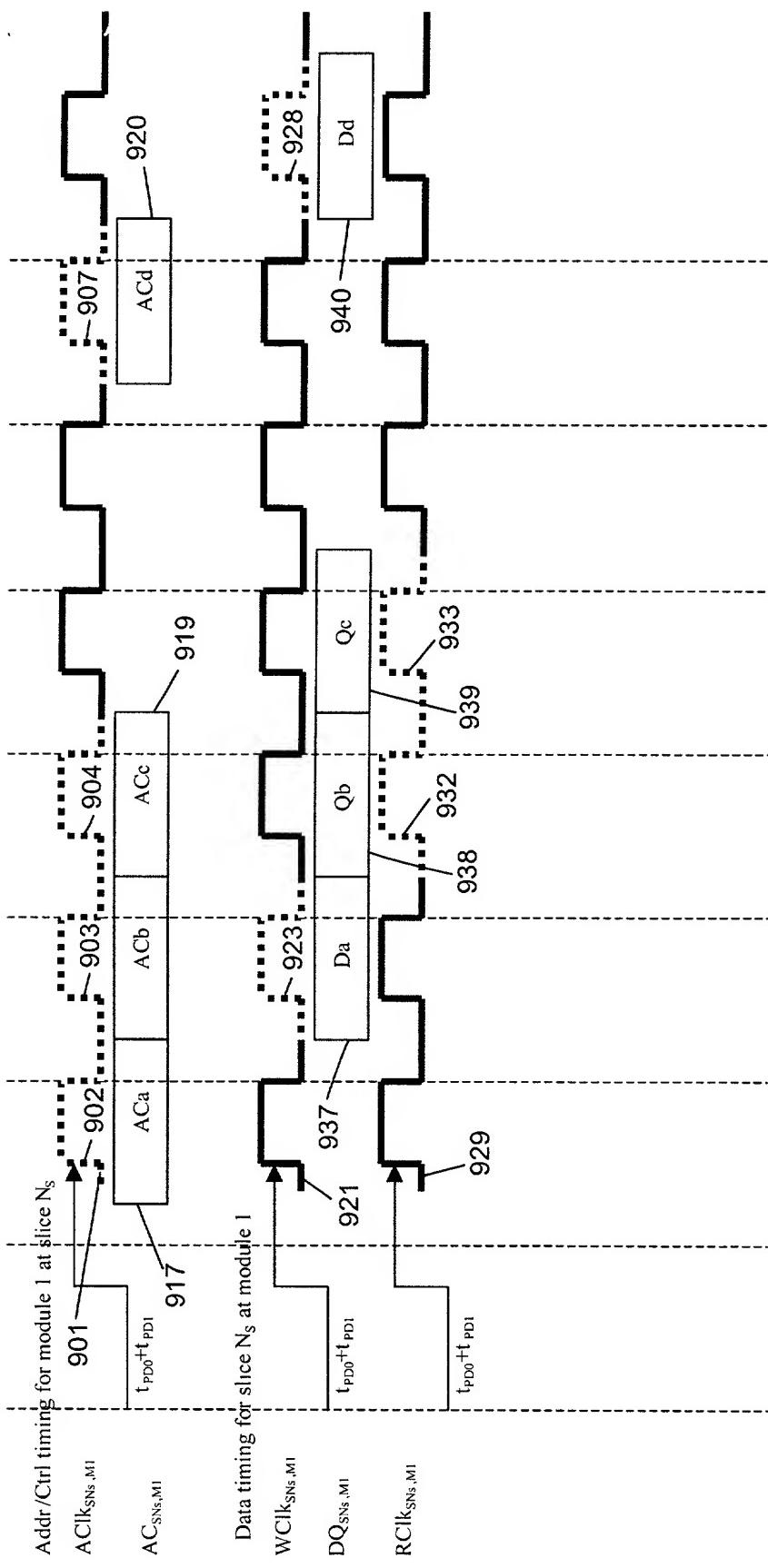


FIG. 10

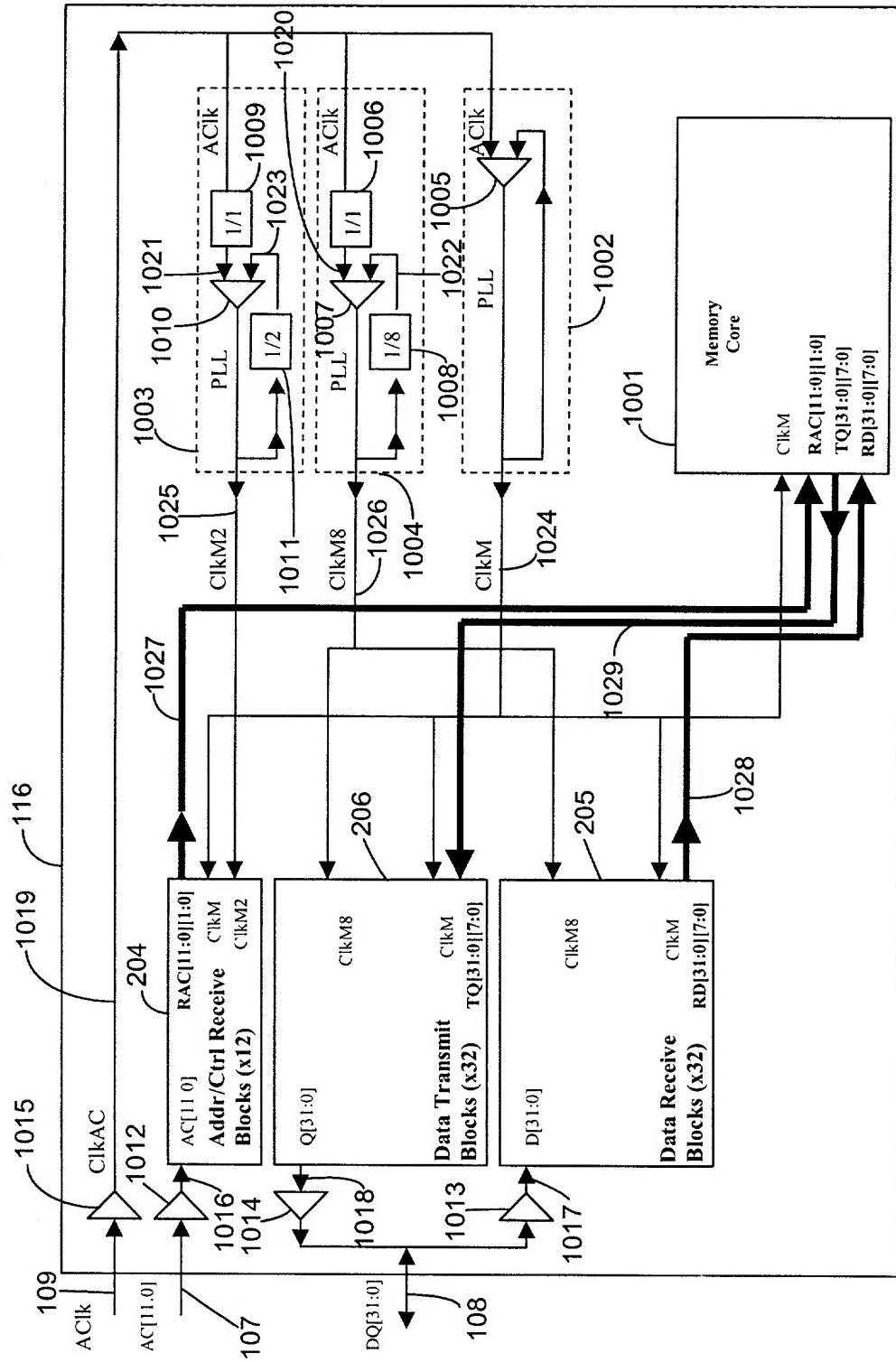


FIG. 11

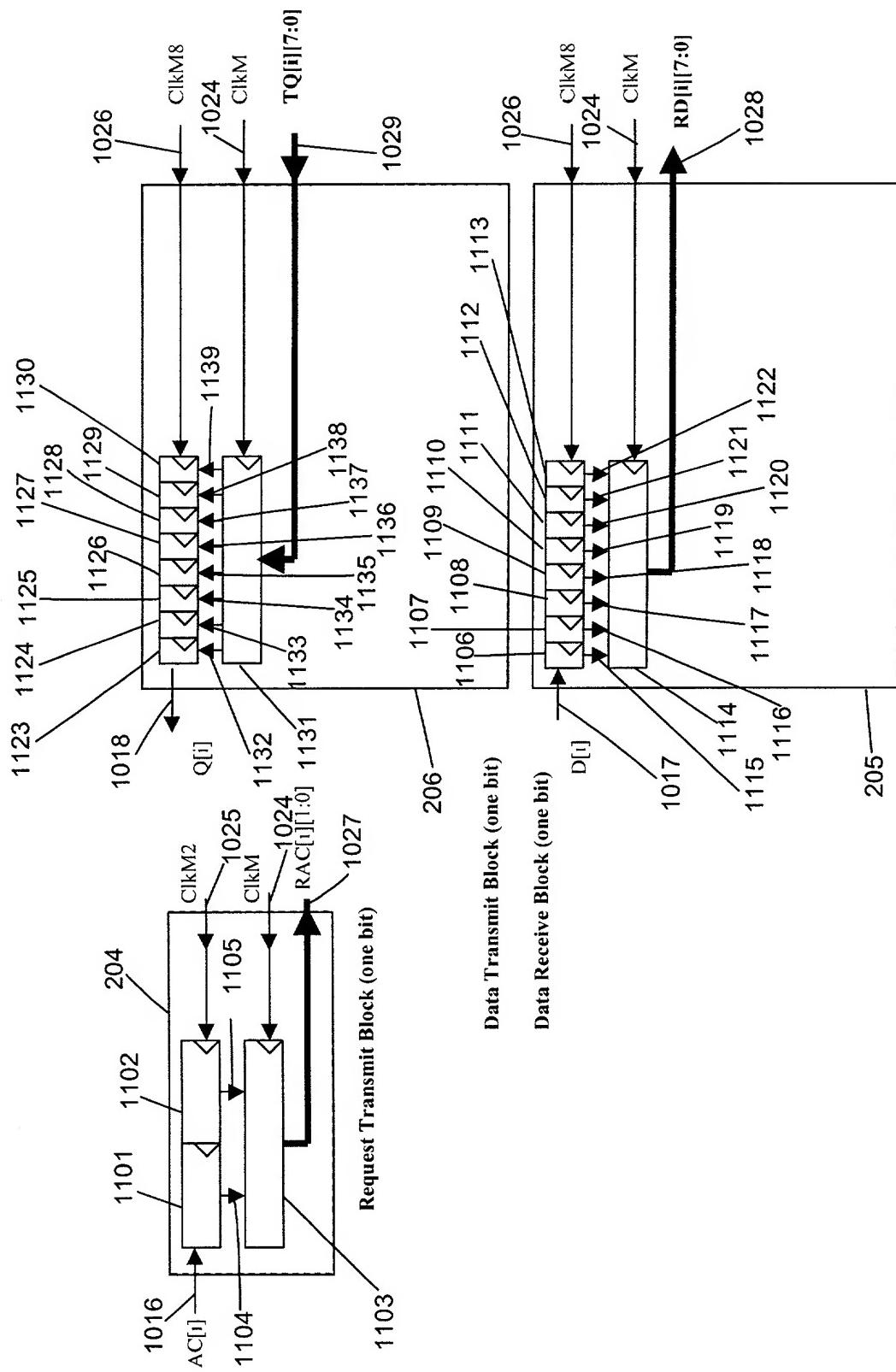
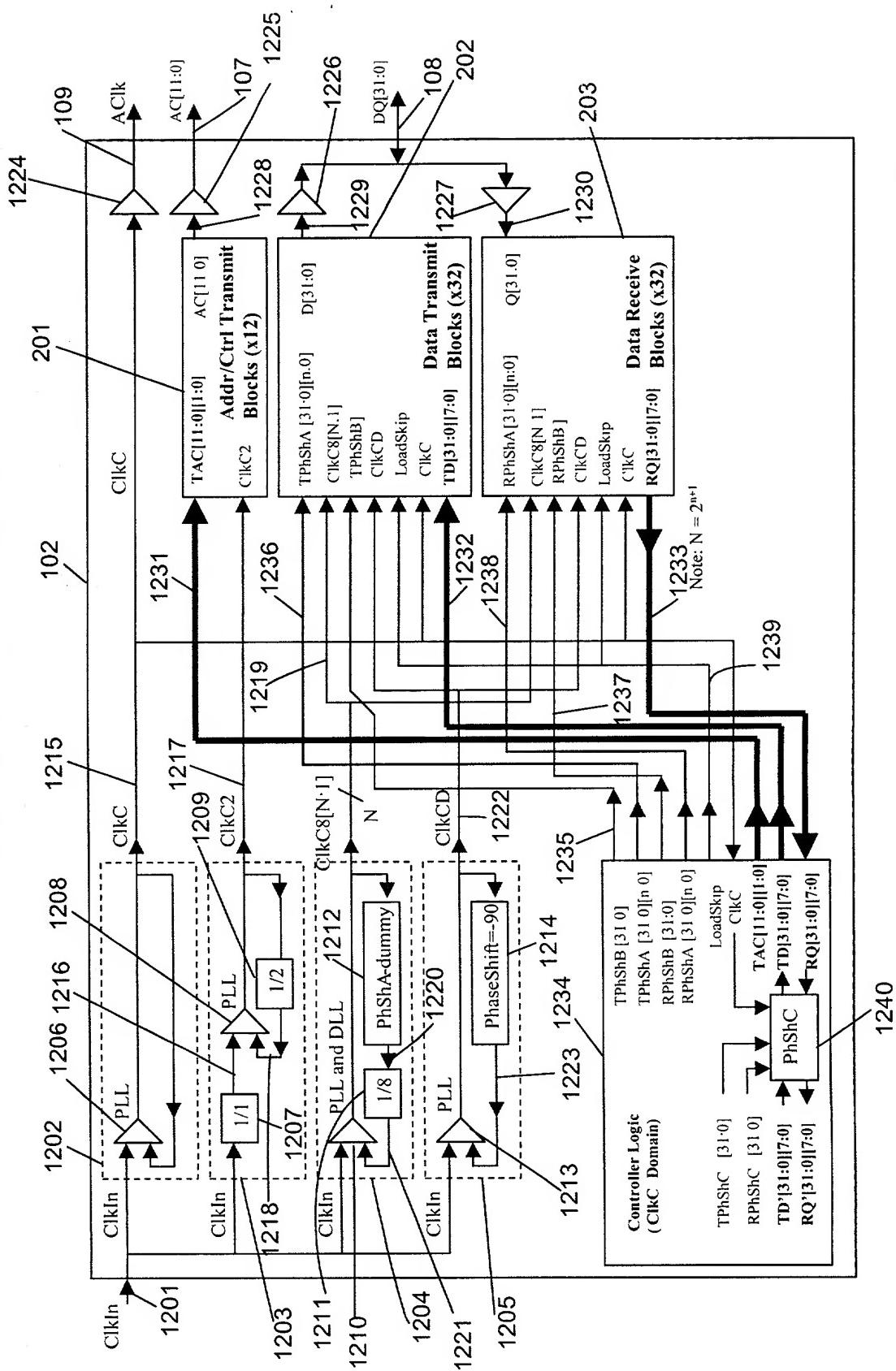


FIG. 12

Figure 12 is a detailed block diagram of a digital signal processing system, likely a memory controller or interface, showing various functional blocks and their connections.



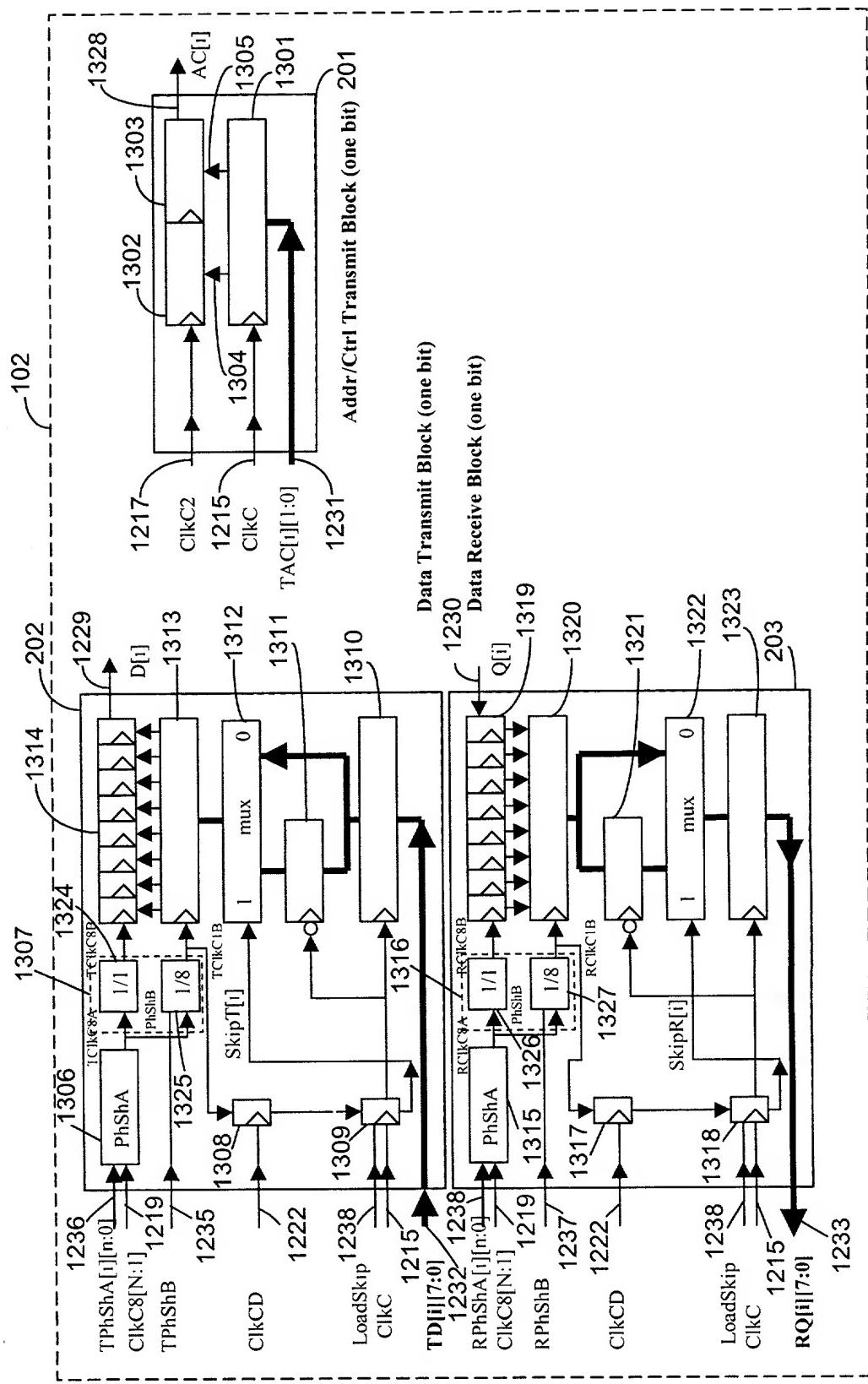


FIG. 13

FIG. 14

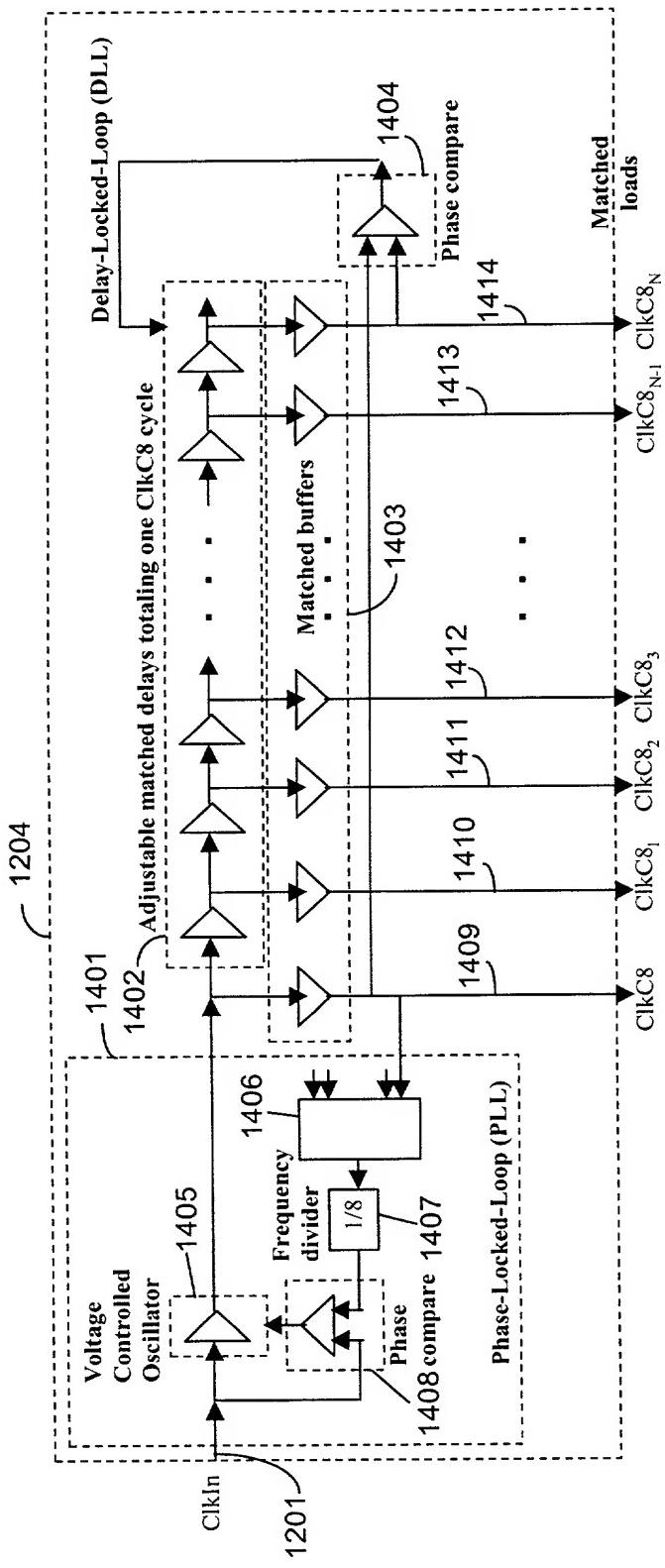


FIG. 15

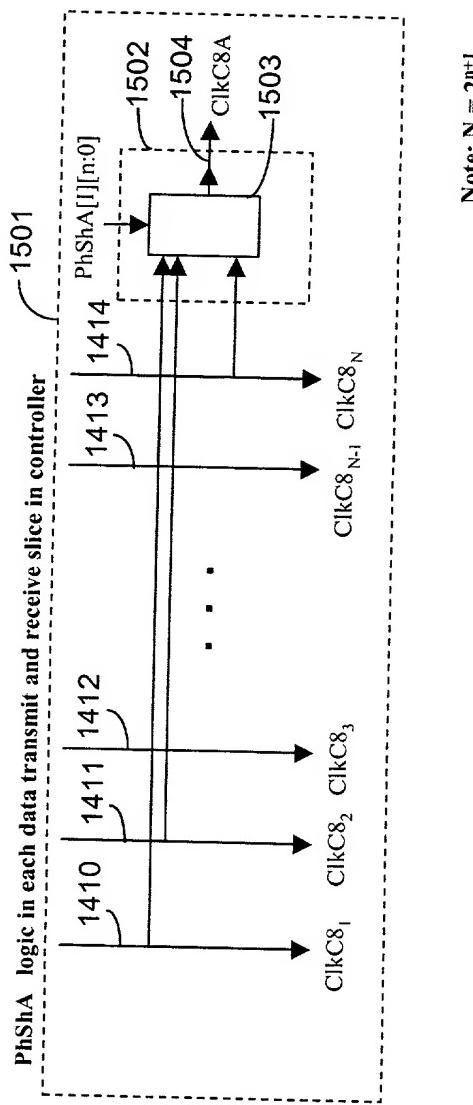
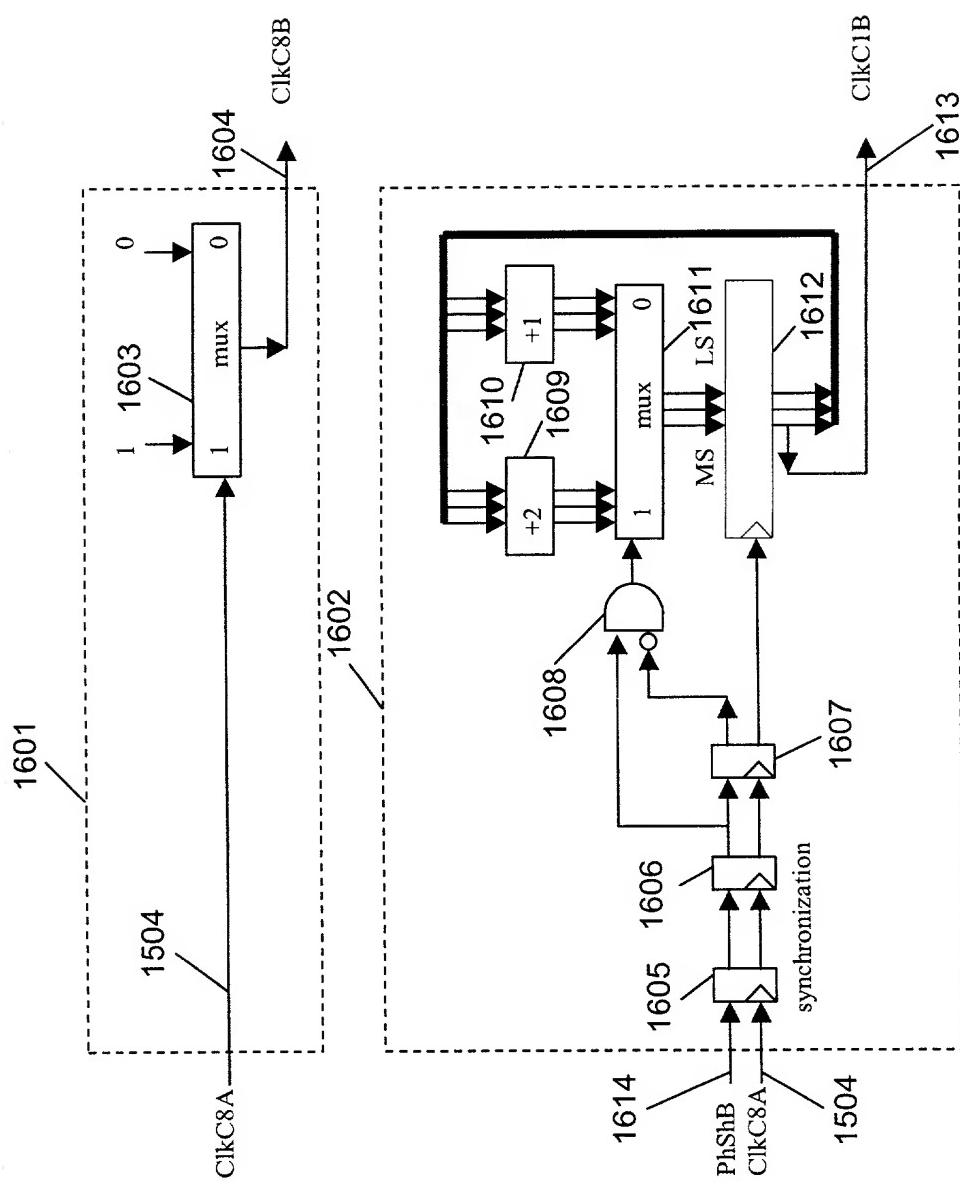


FIG. 16



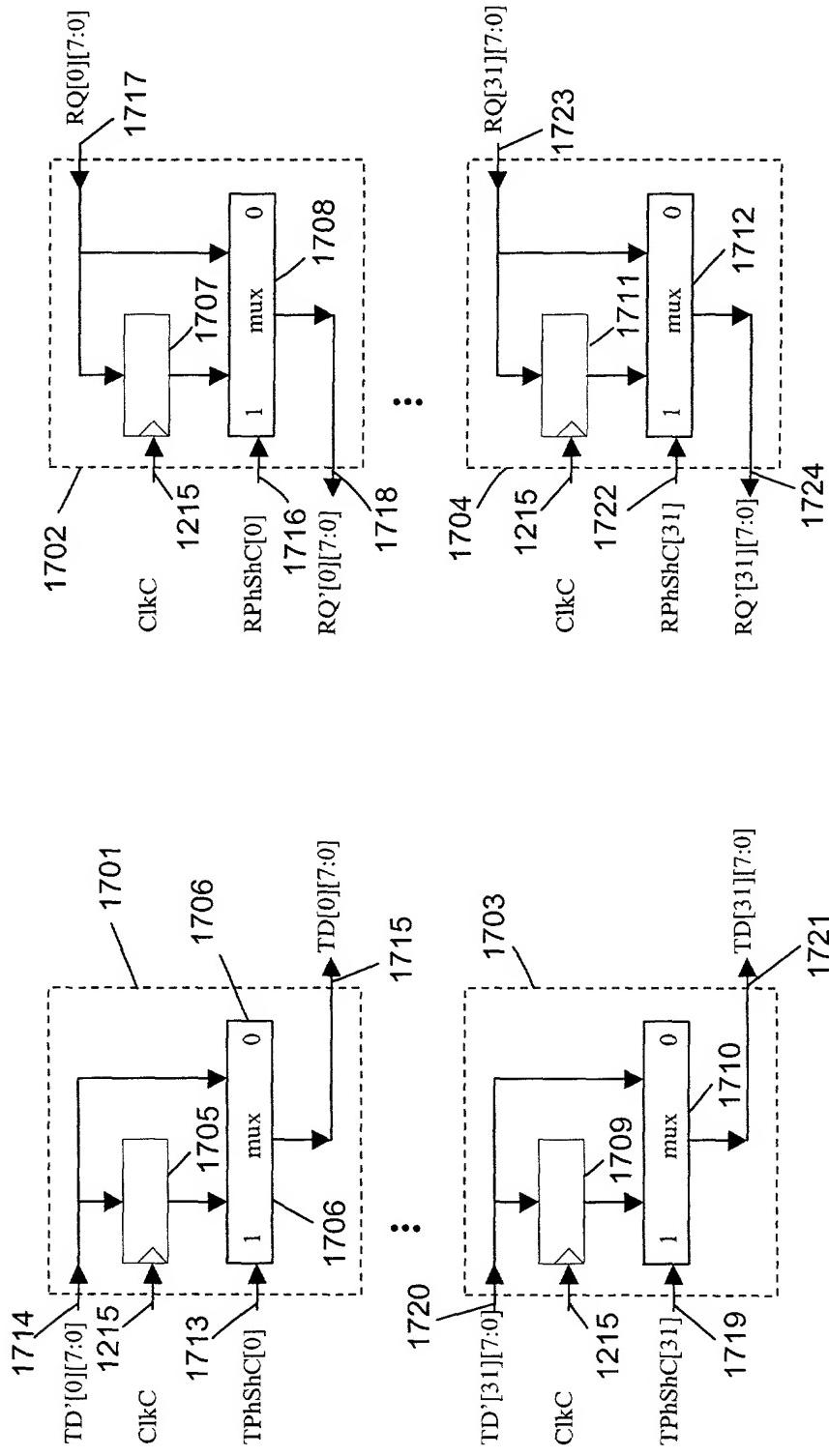
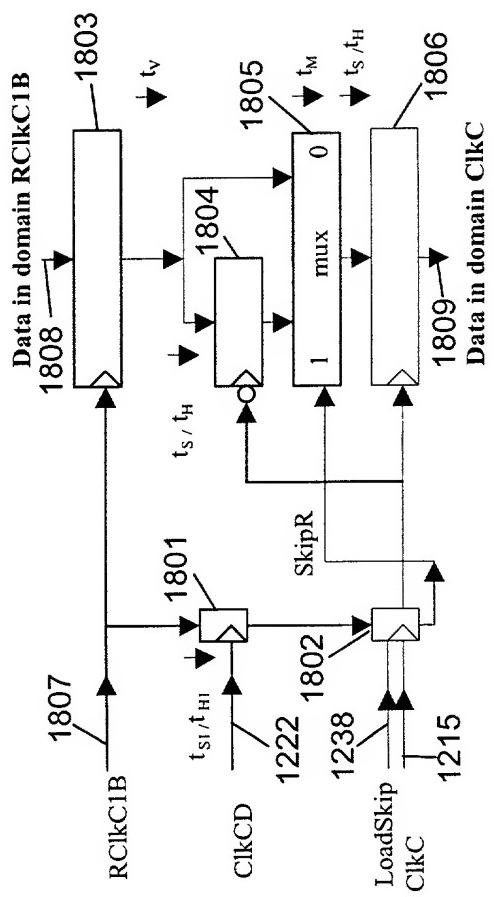


FIG. 17

FIG. 18



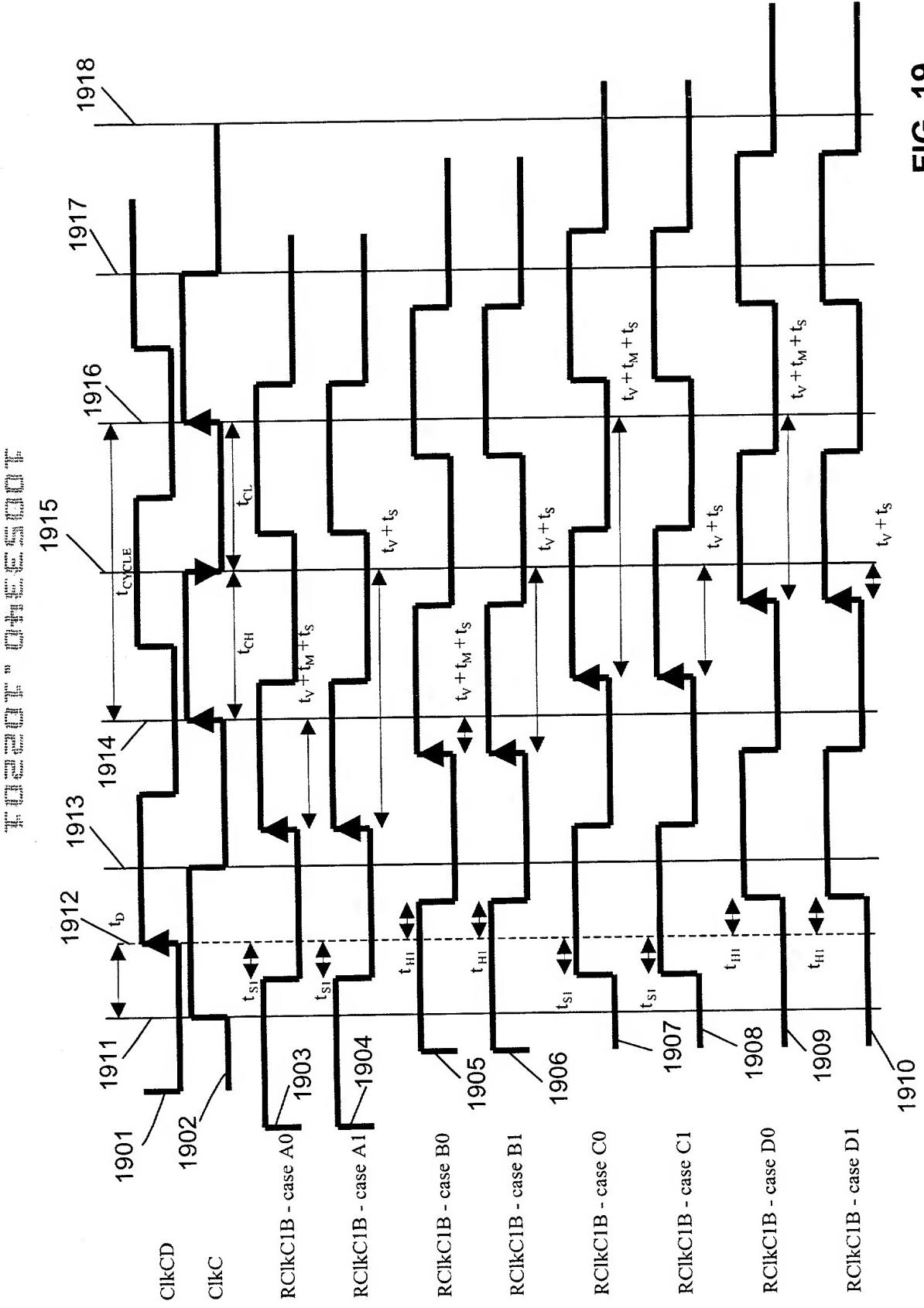


FIG. 19

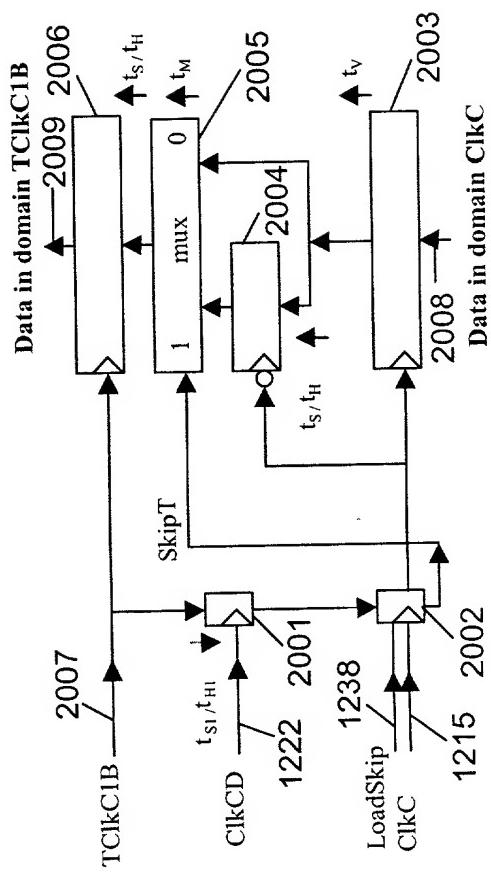


FIG. 20

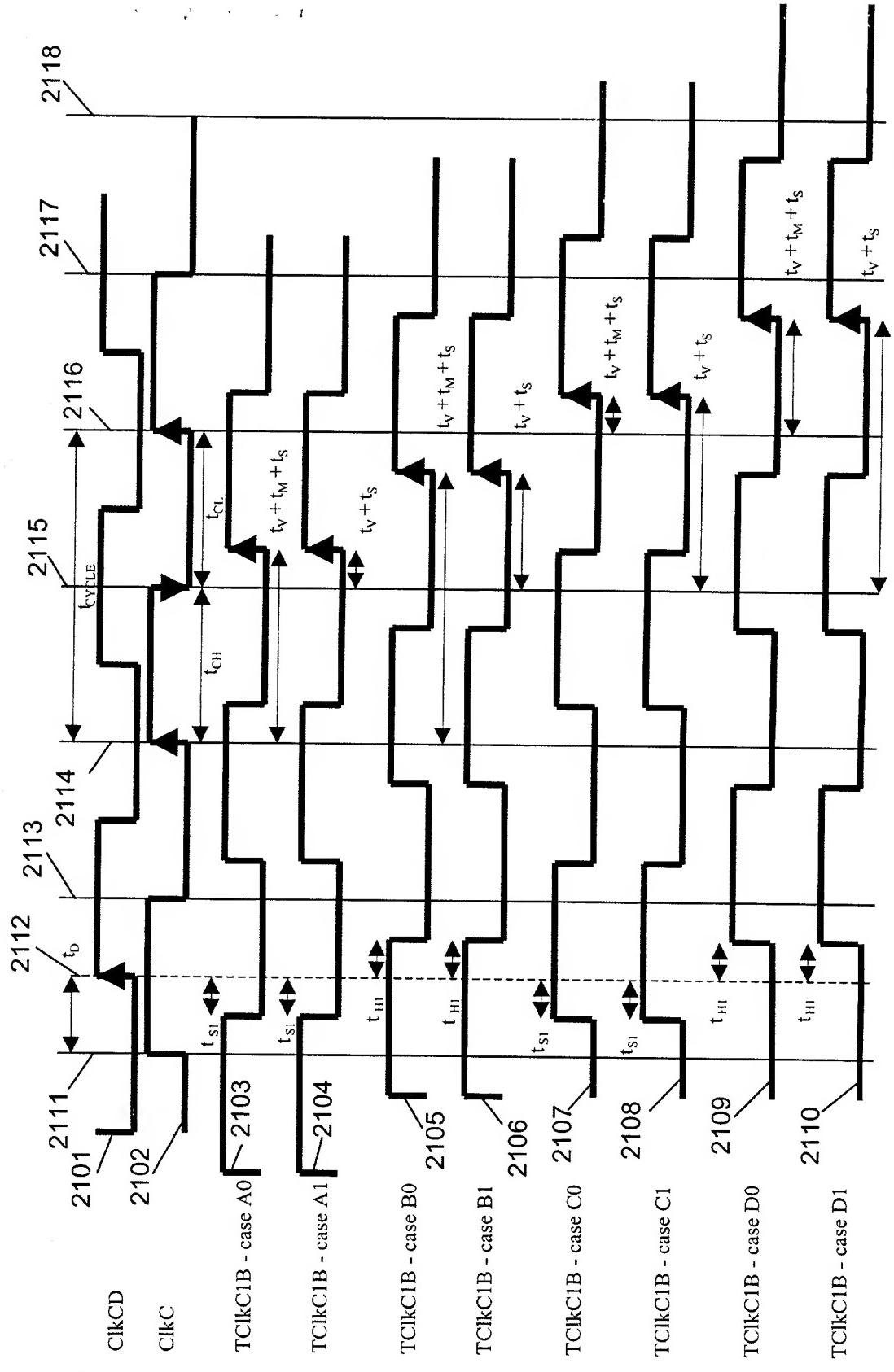
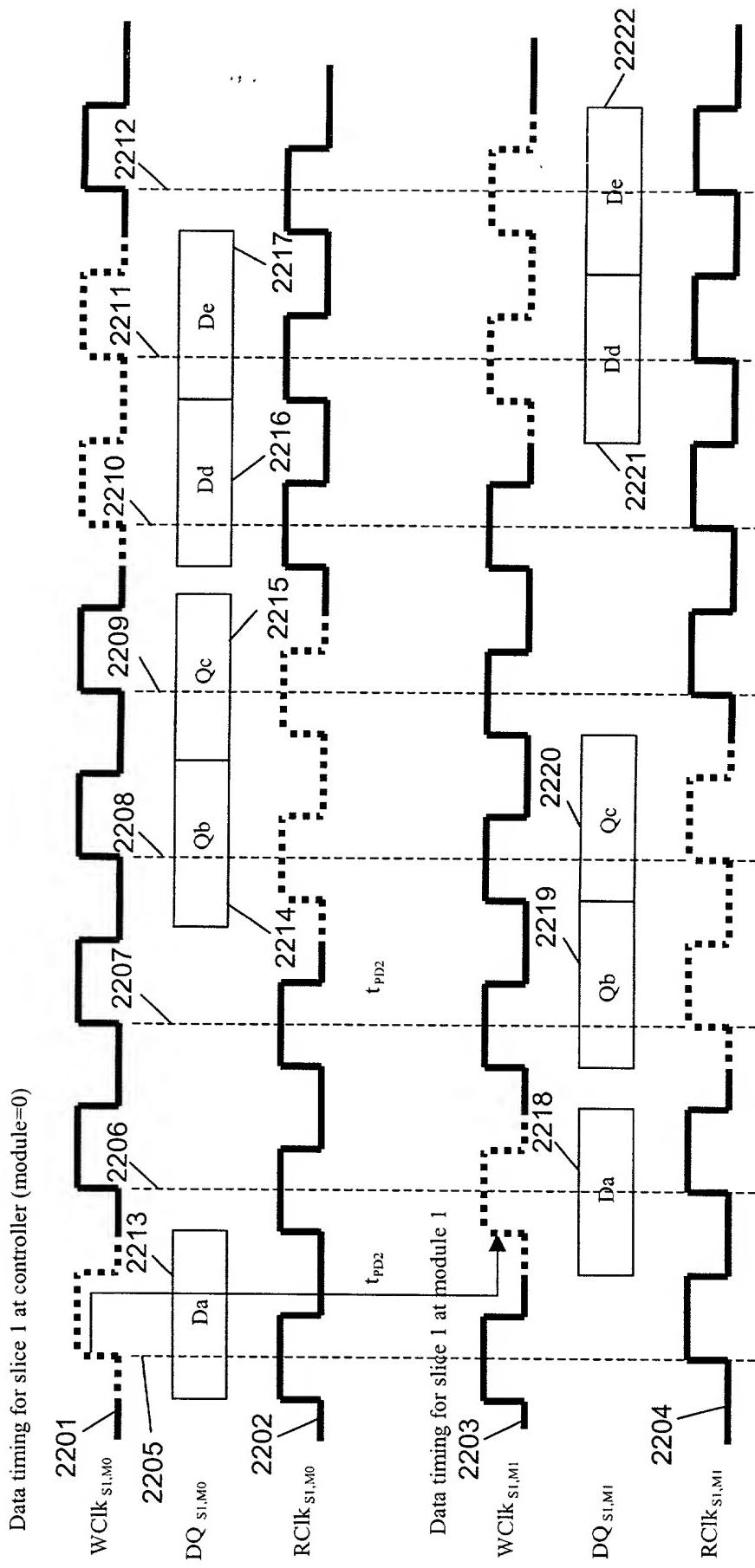


FIG. 21

FIG. 22



Data timing for slice 1 at controller (module=0)

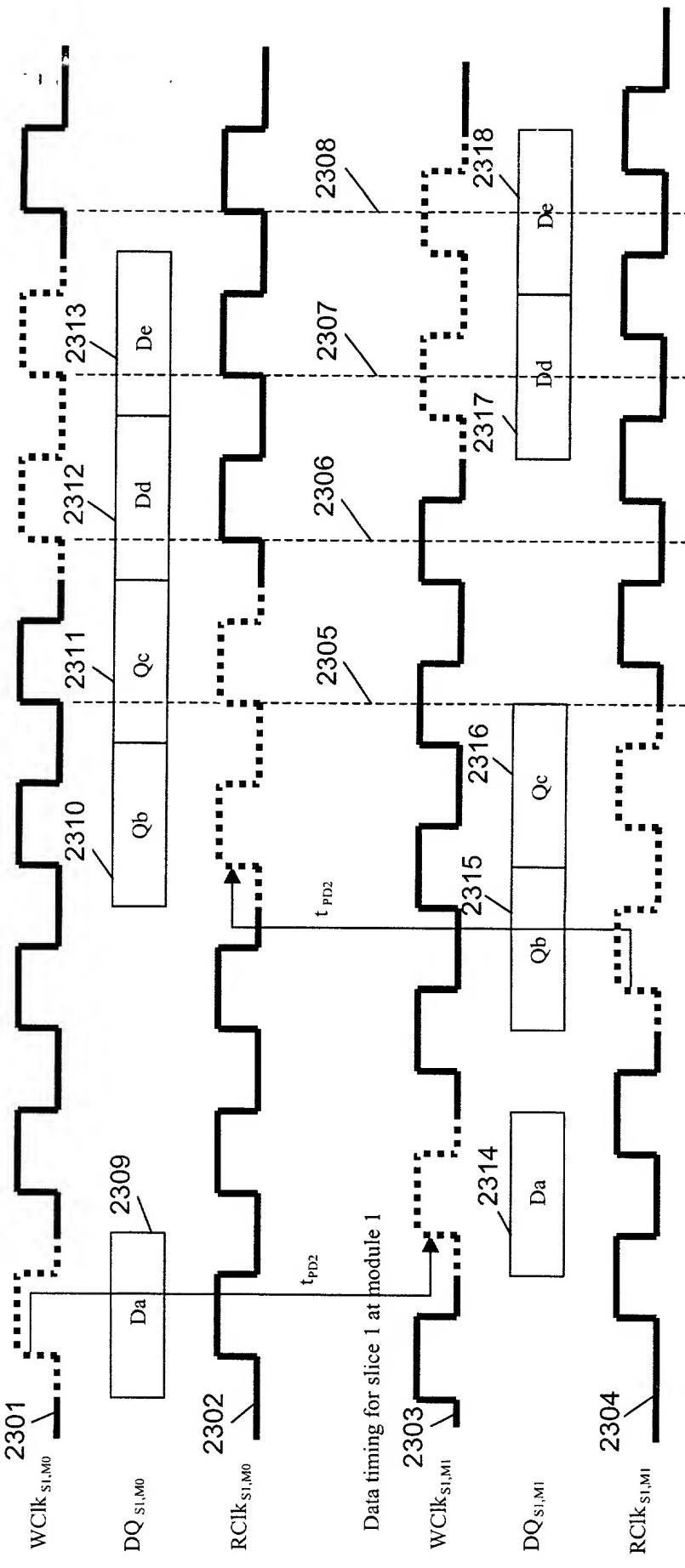


FIG. 23

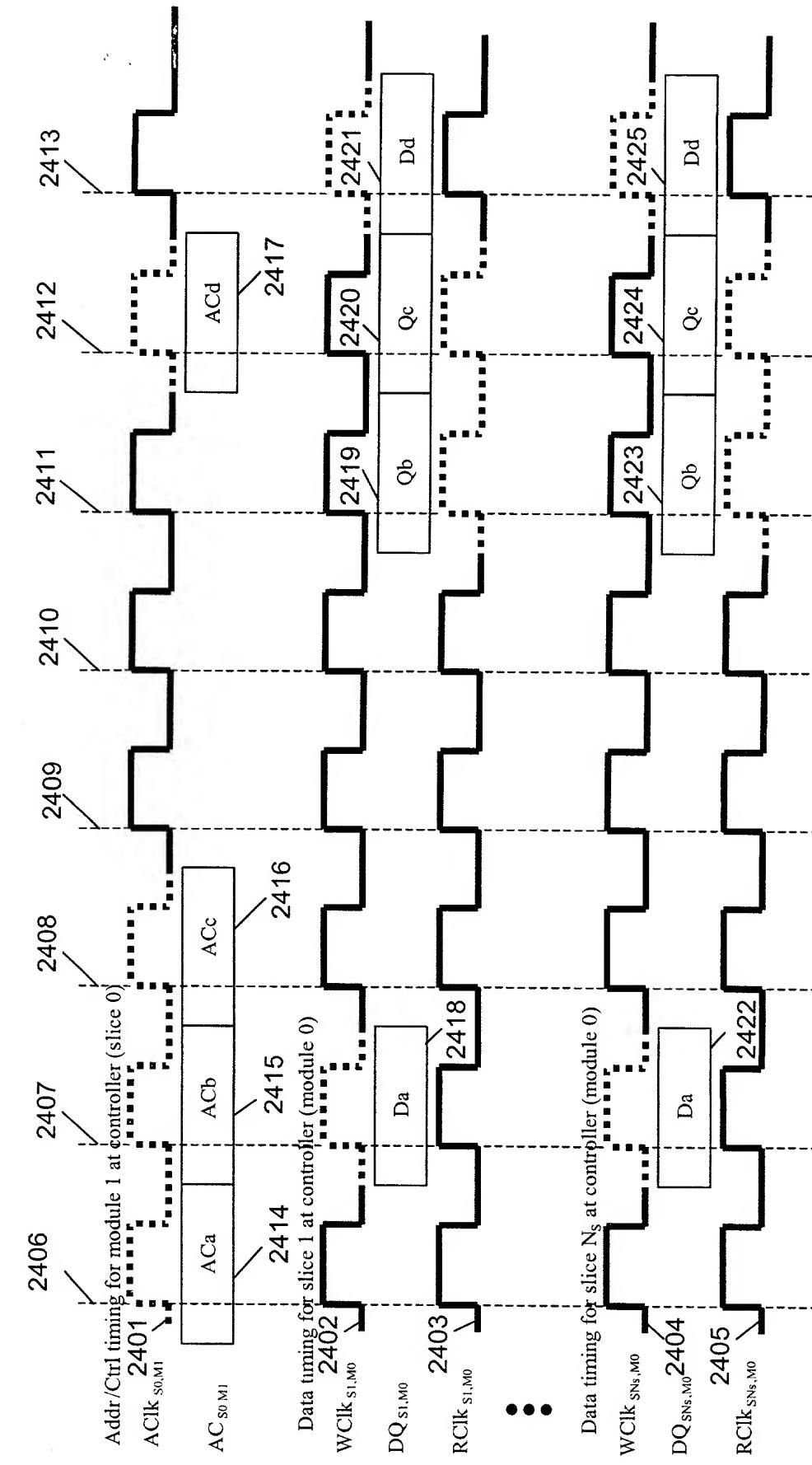


FIG. 24

FIG. 25

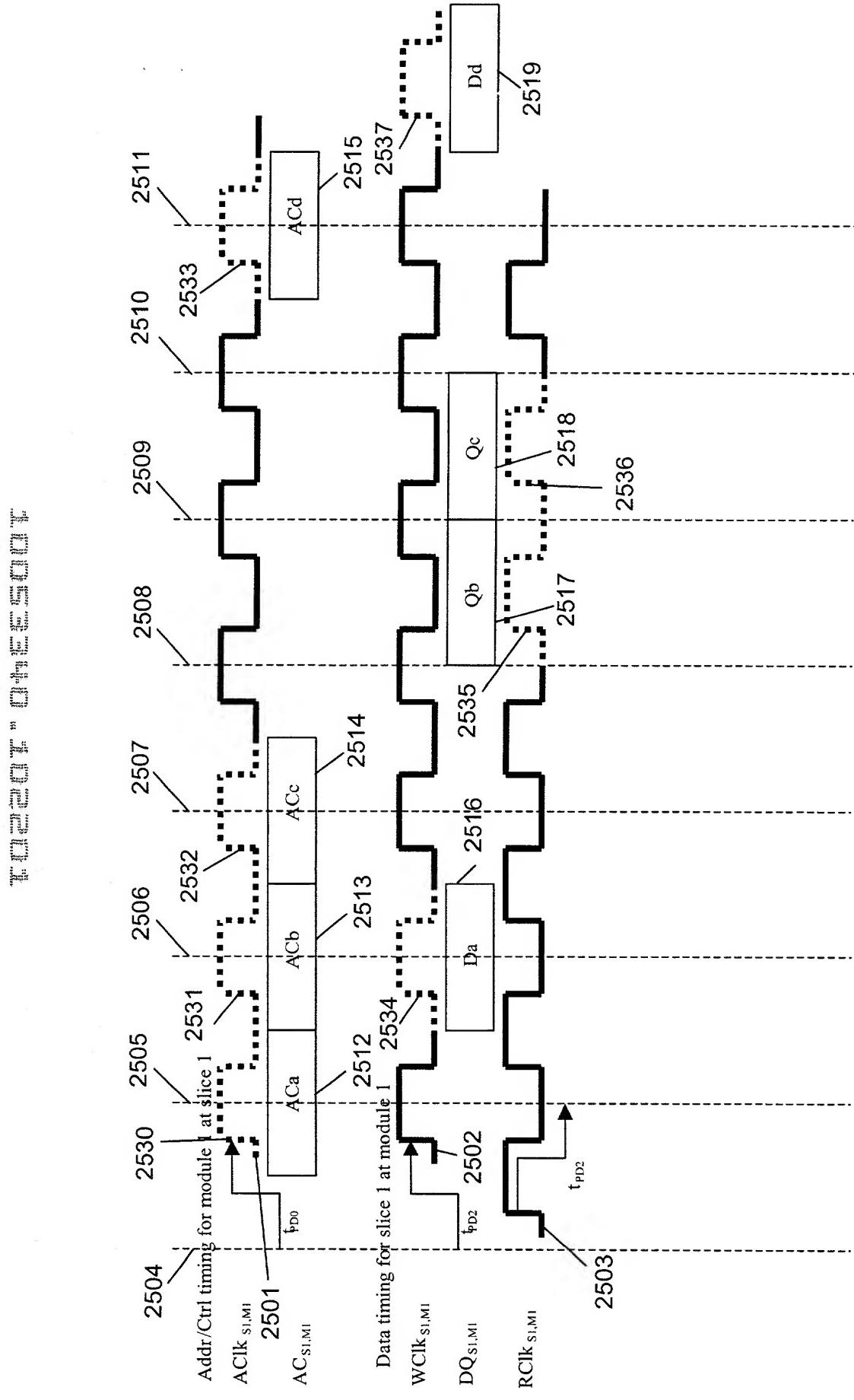


FIG. 26

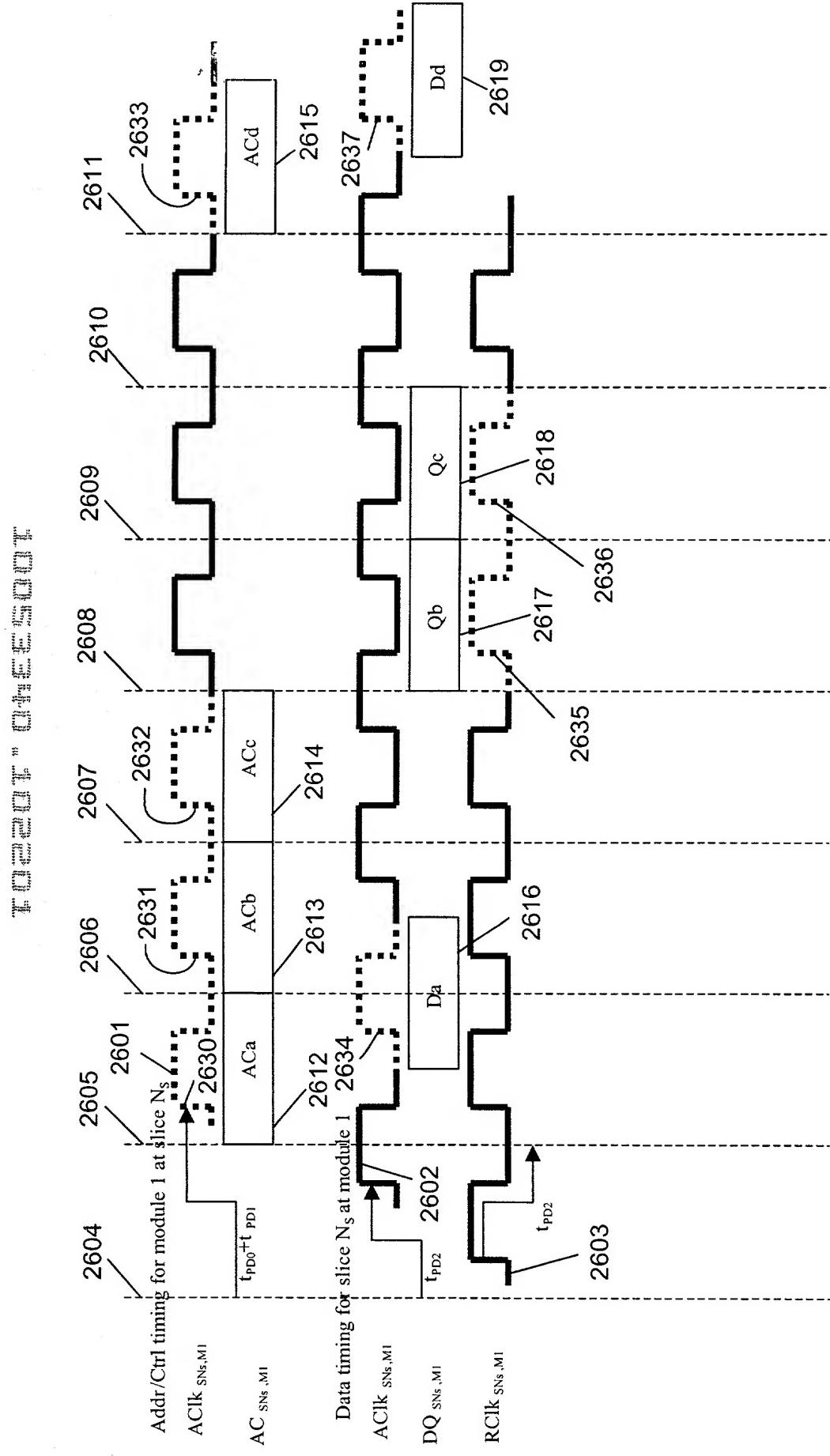
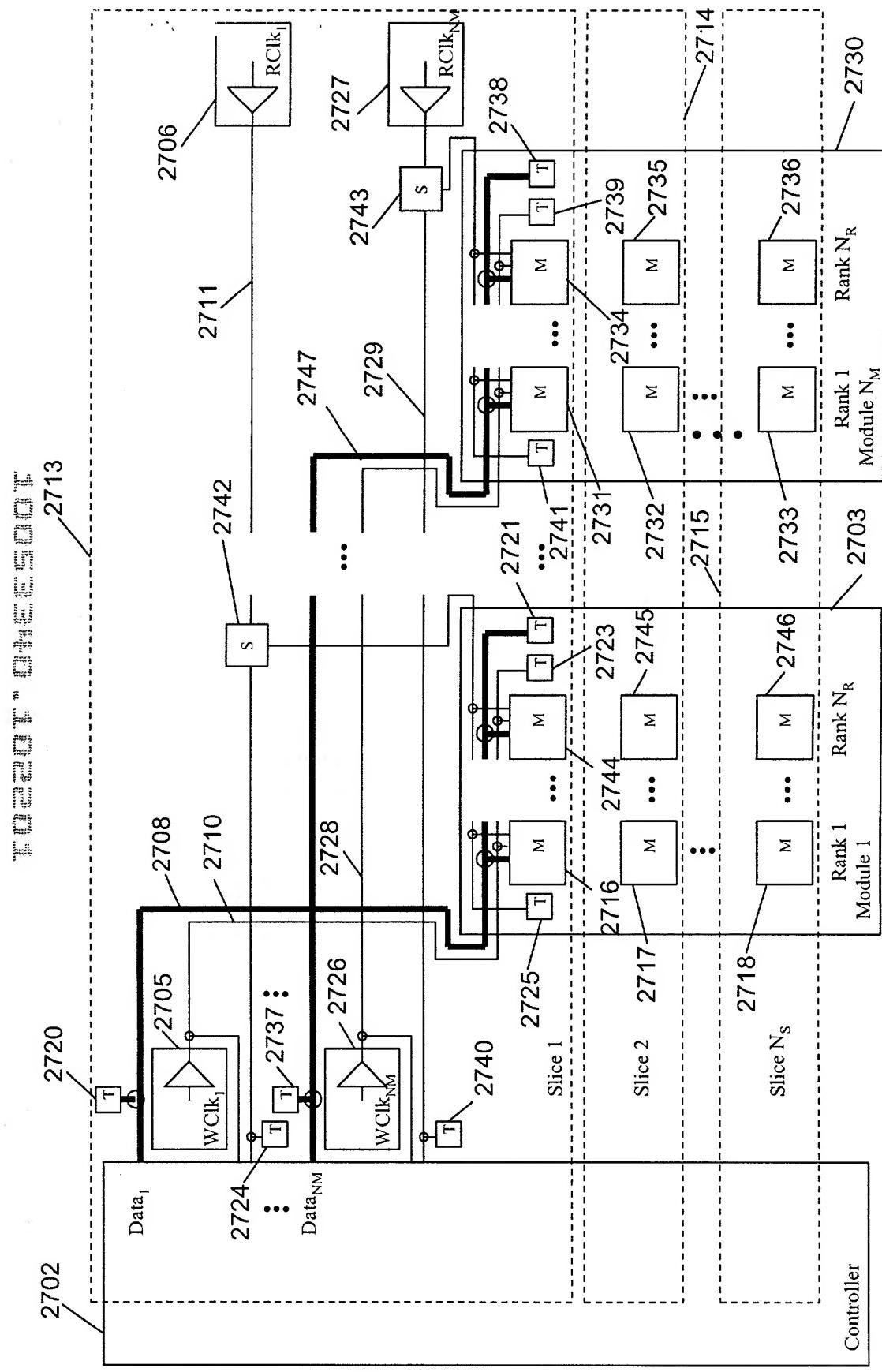


FIG. 27



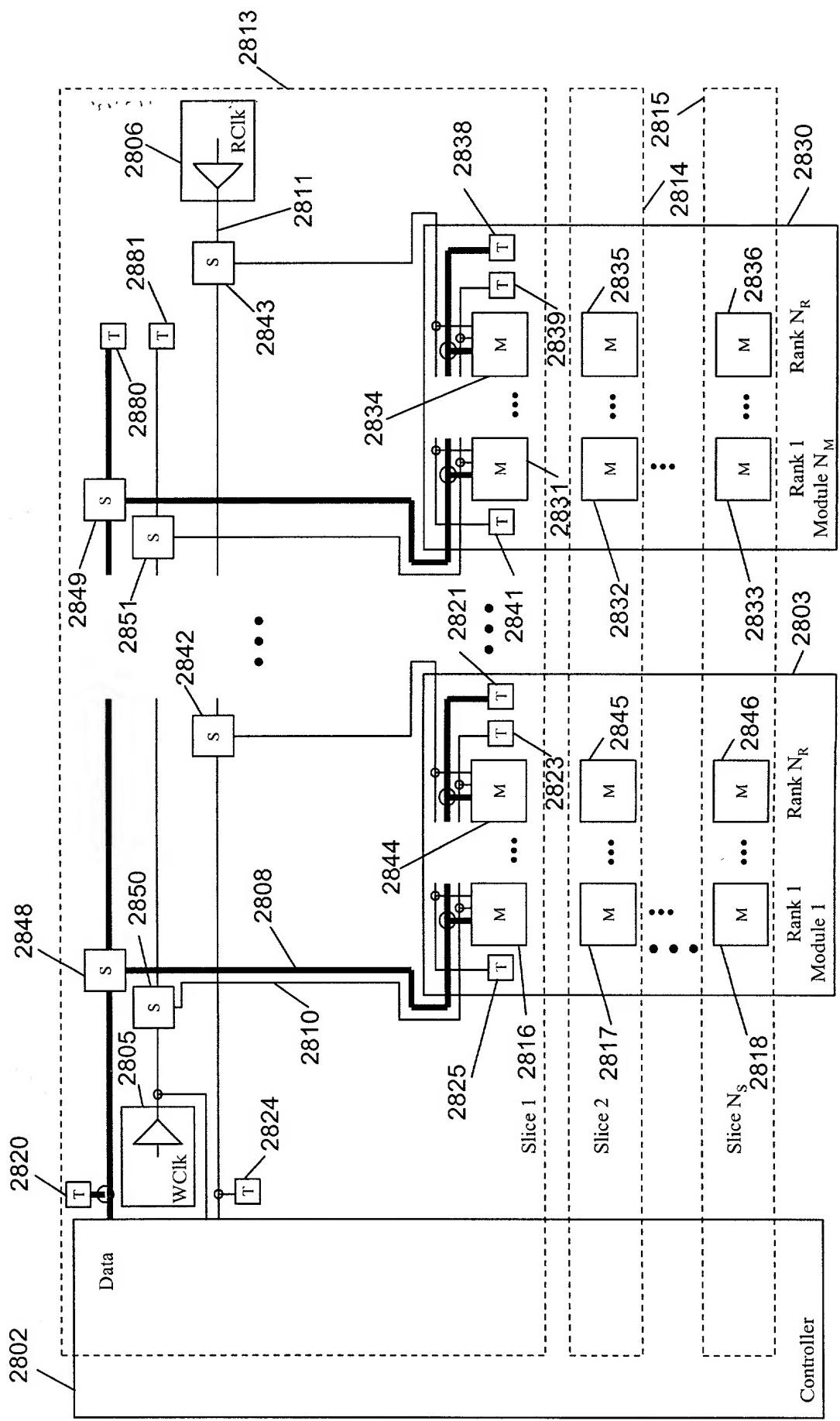


FIG. 28

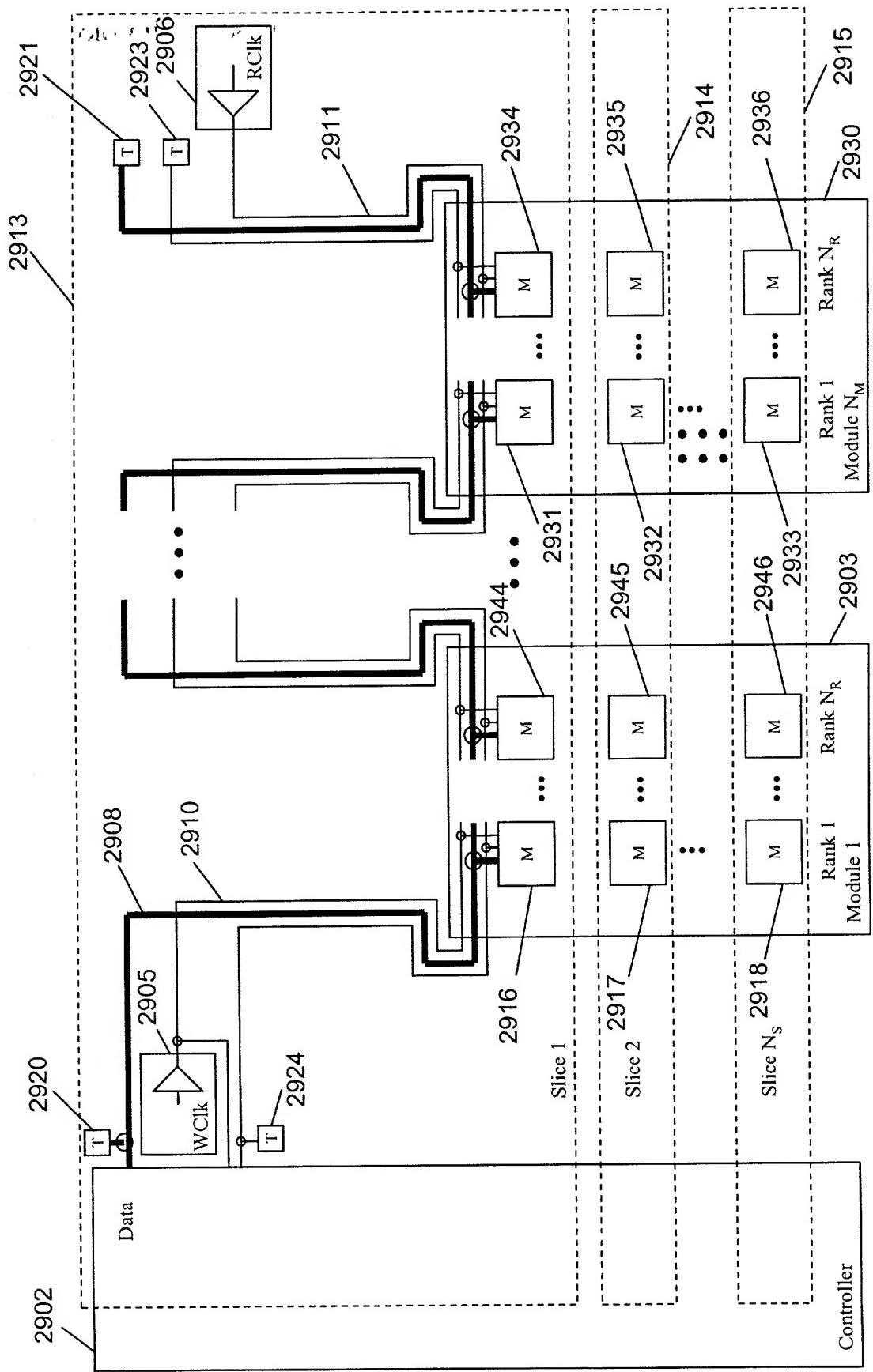


FIG. 29

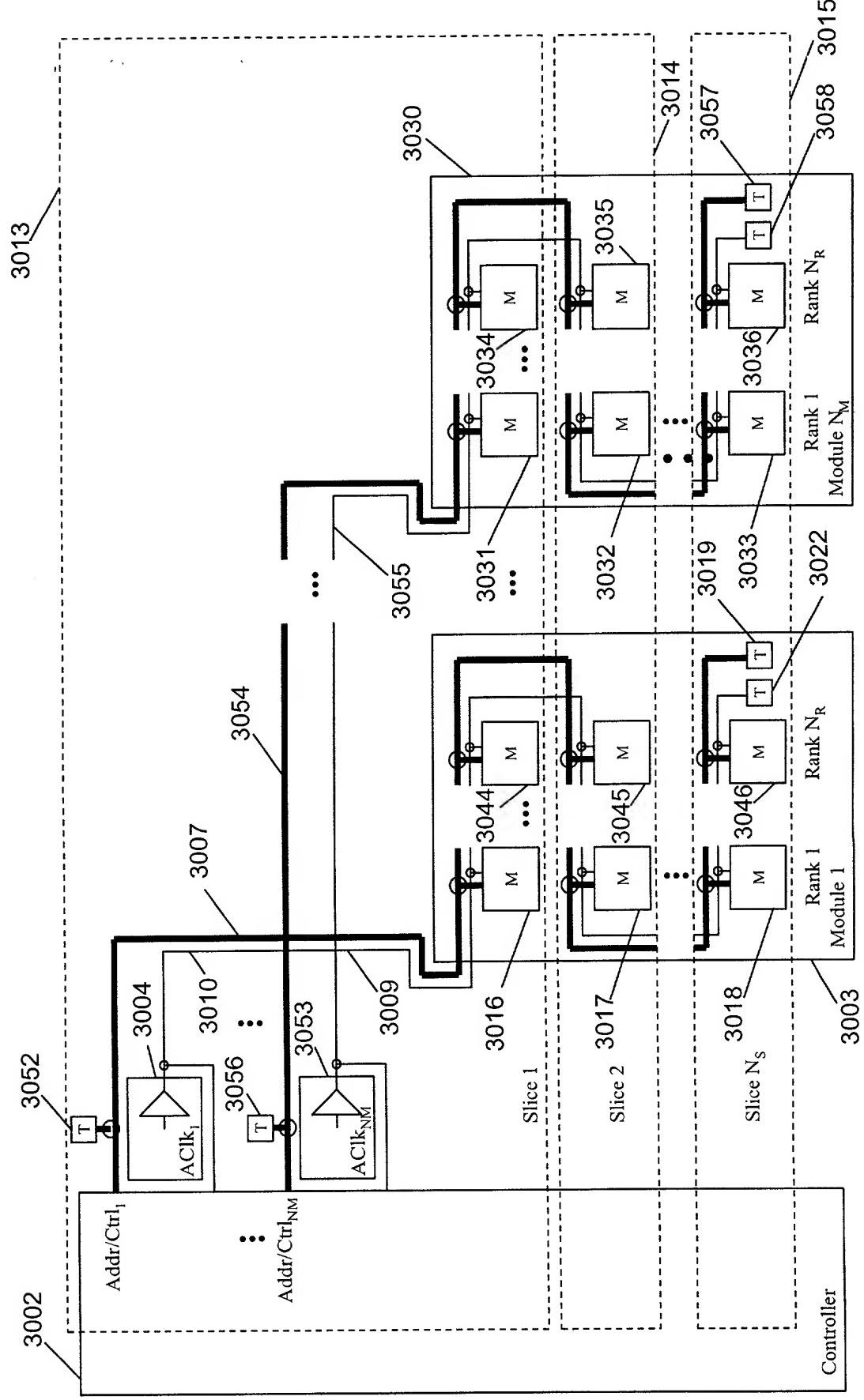


FIG. 30

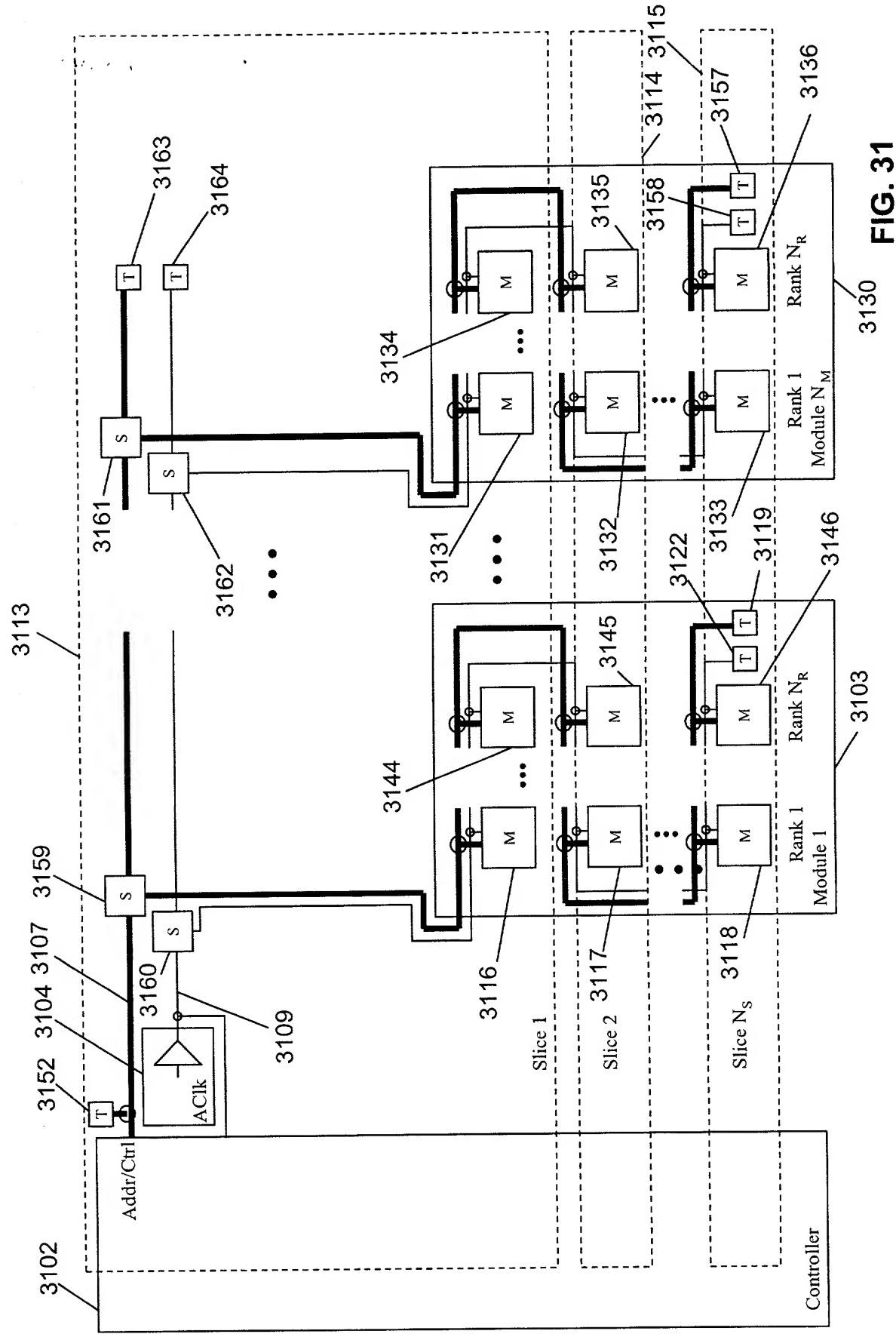


FIG. 31

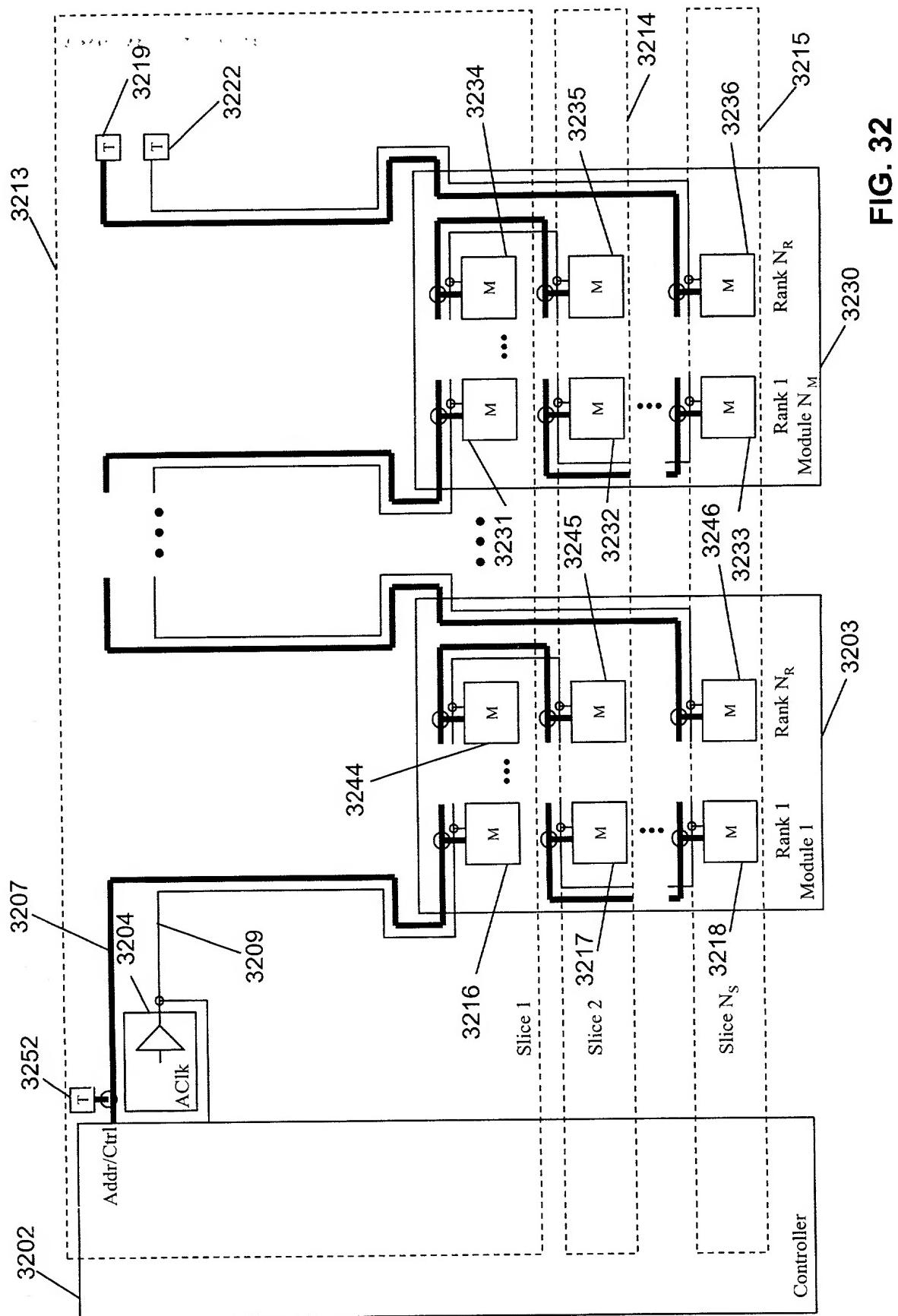


FIG. 32

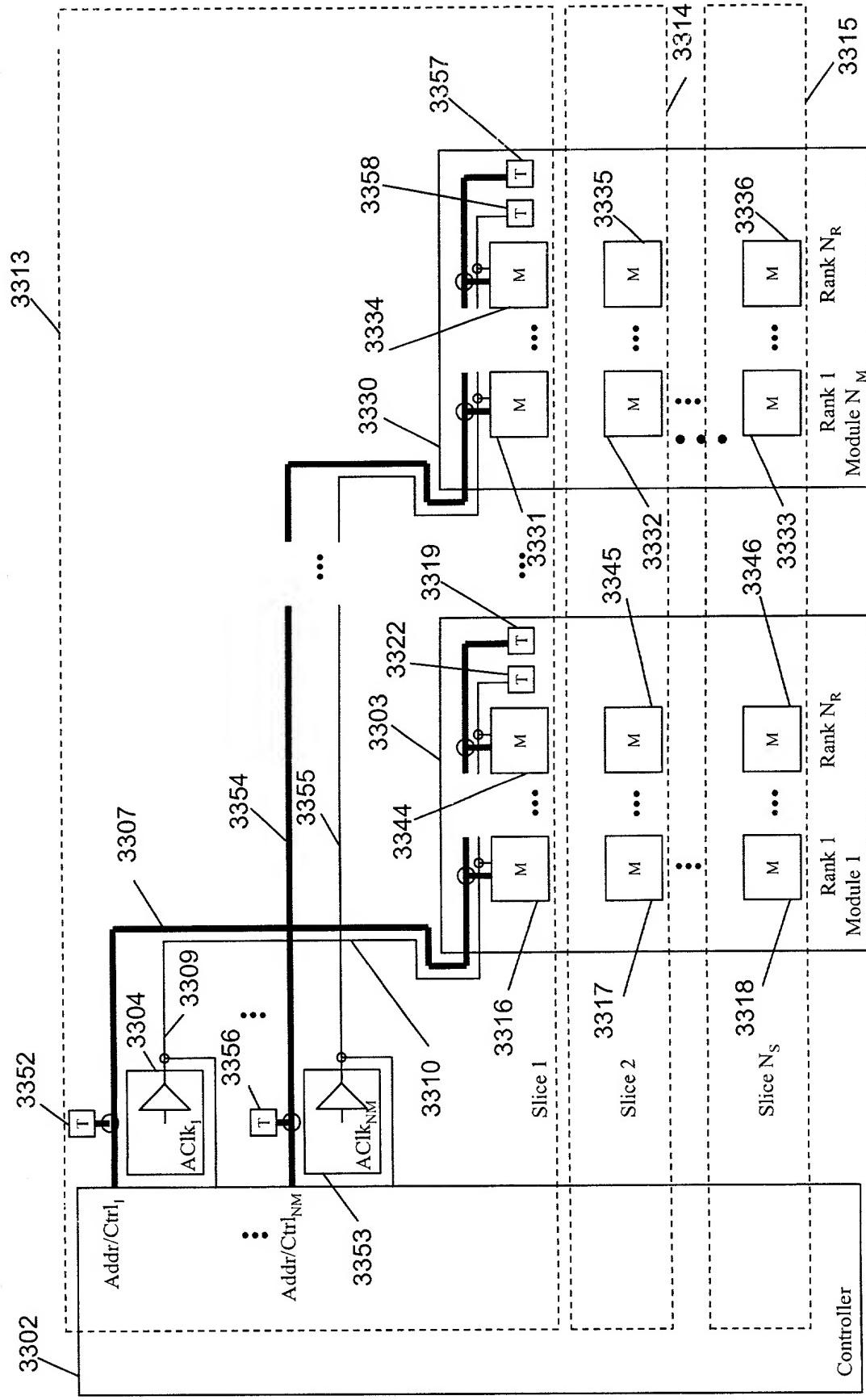


FIG. 33

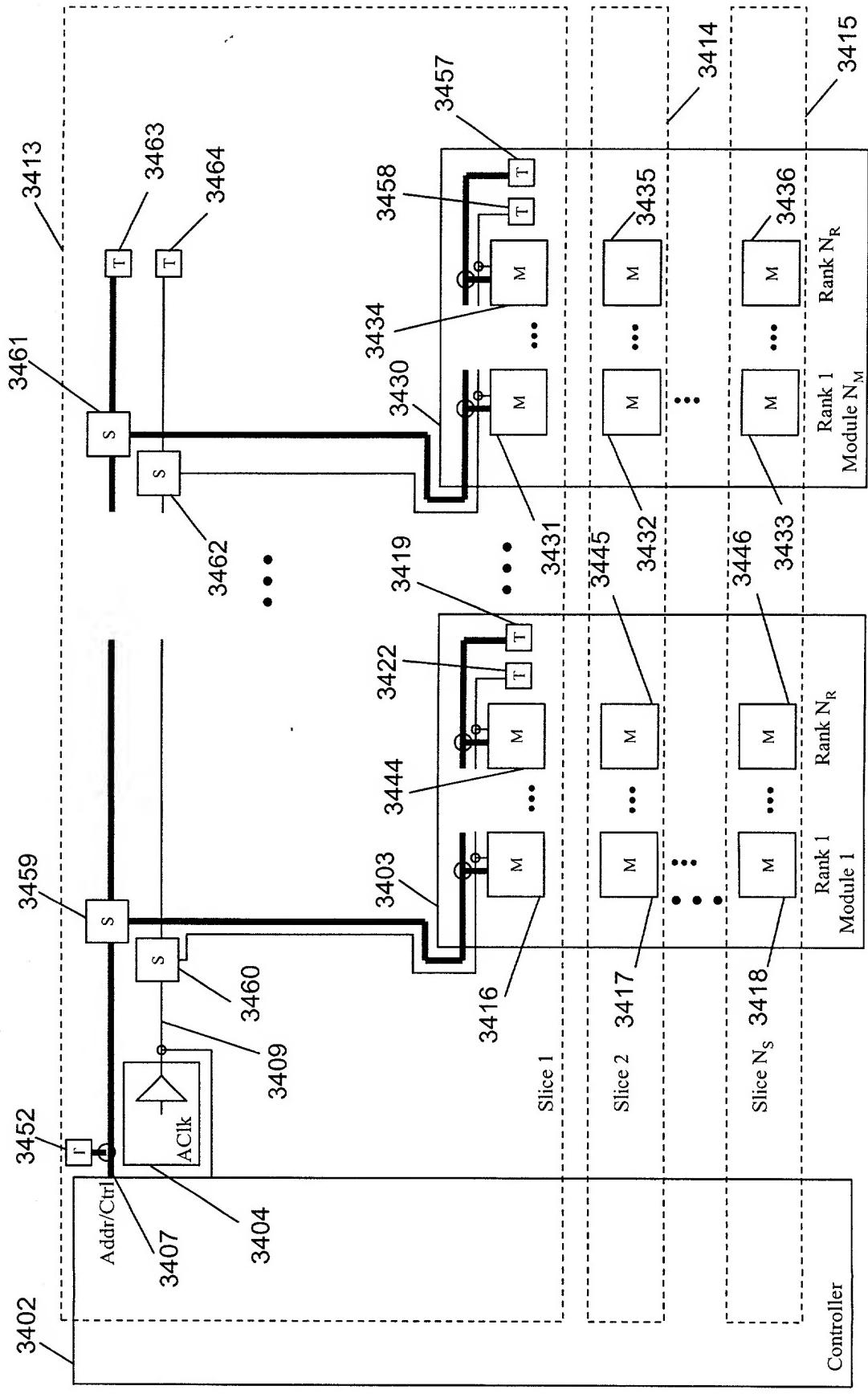


FIG. 34

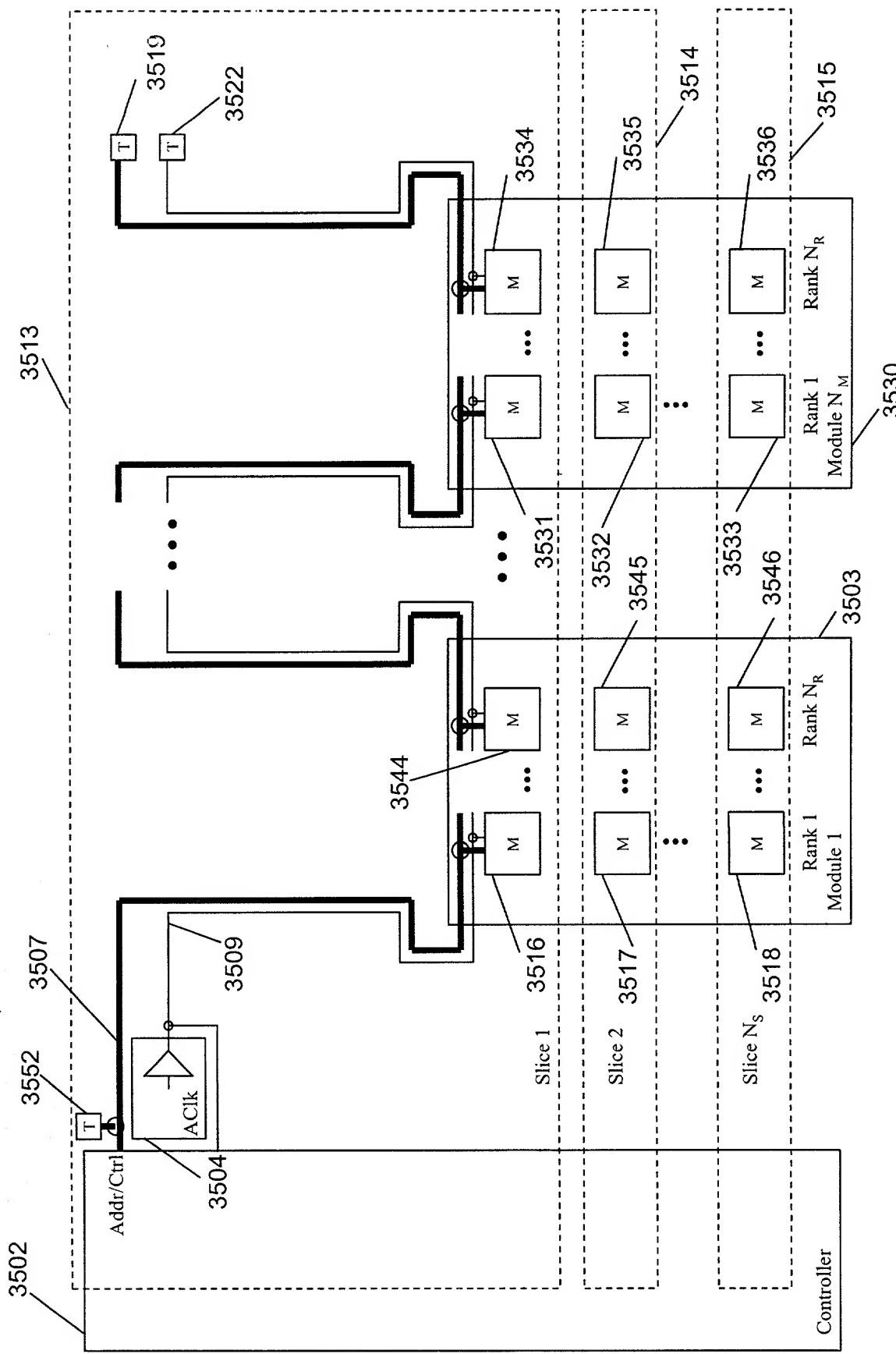
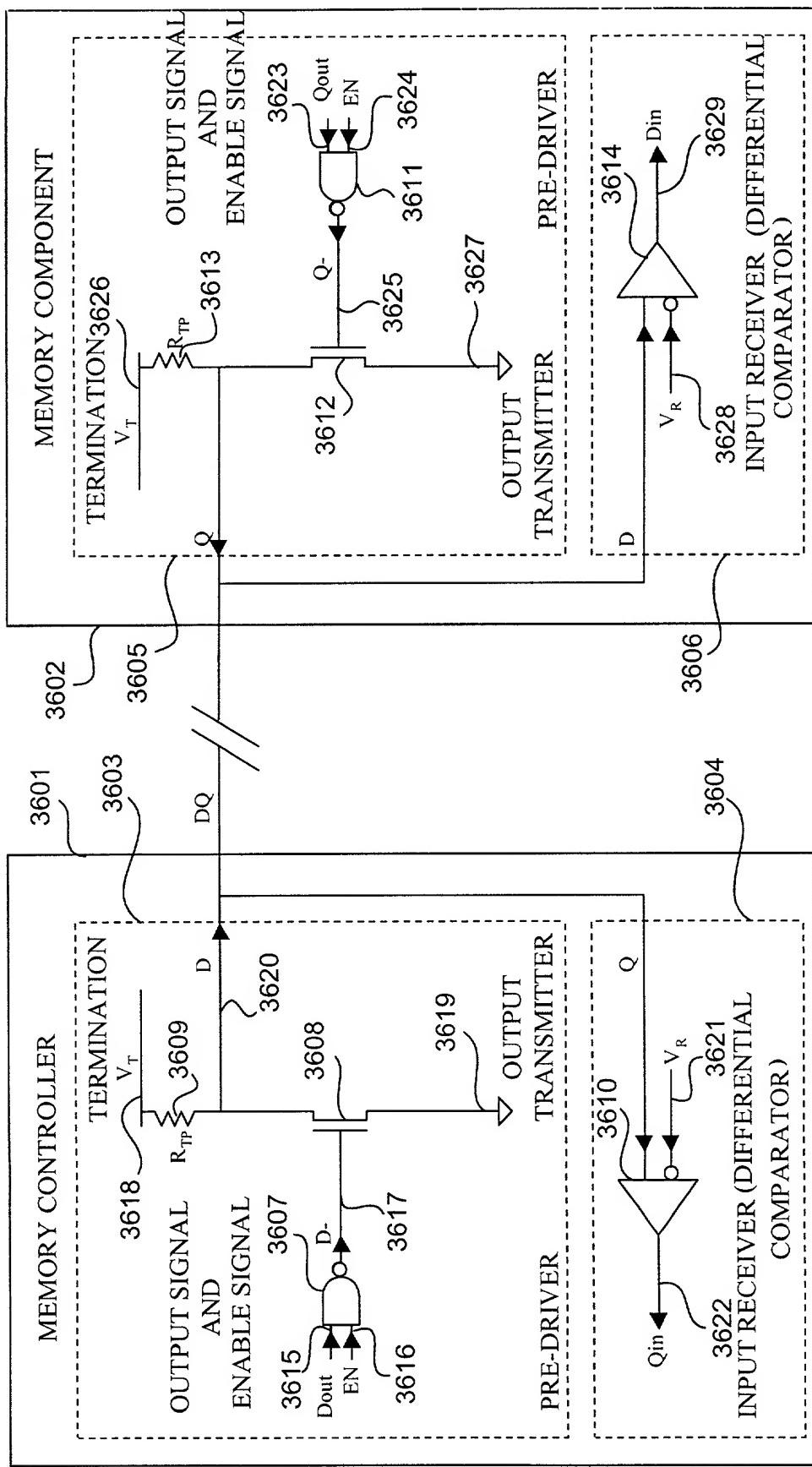


FIG. 35

FIG. 36



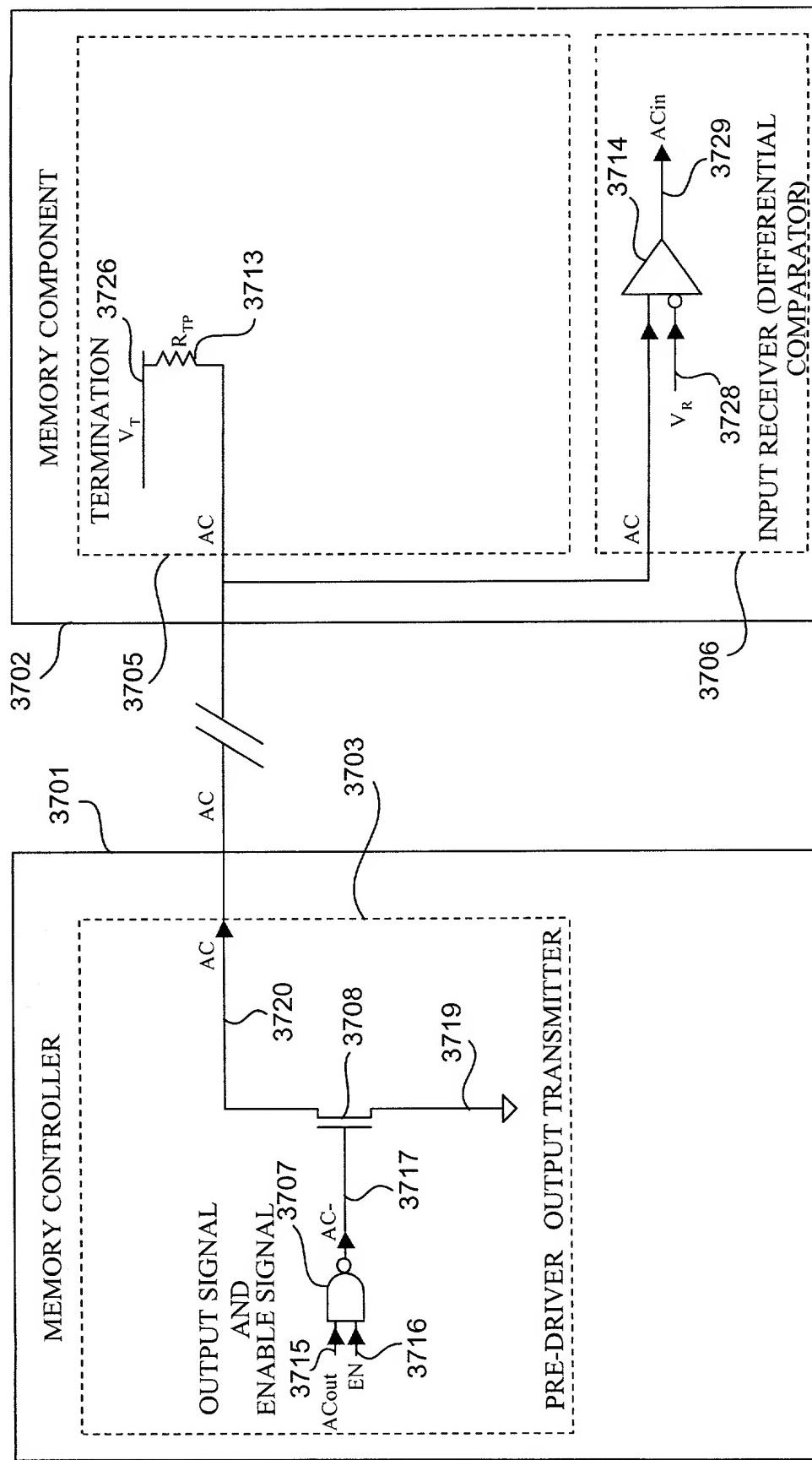
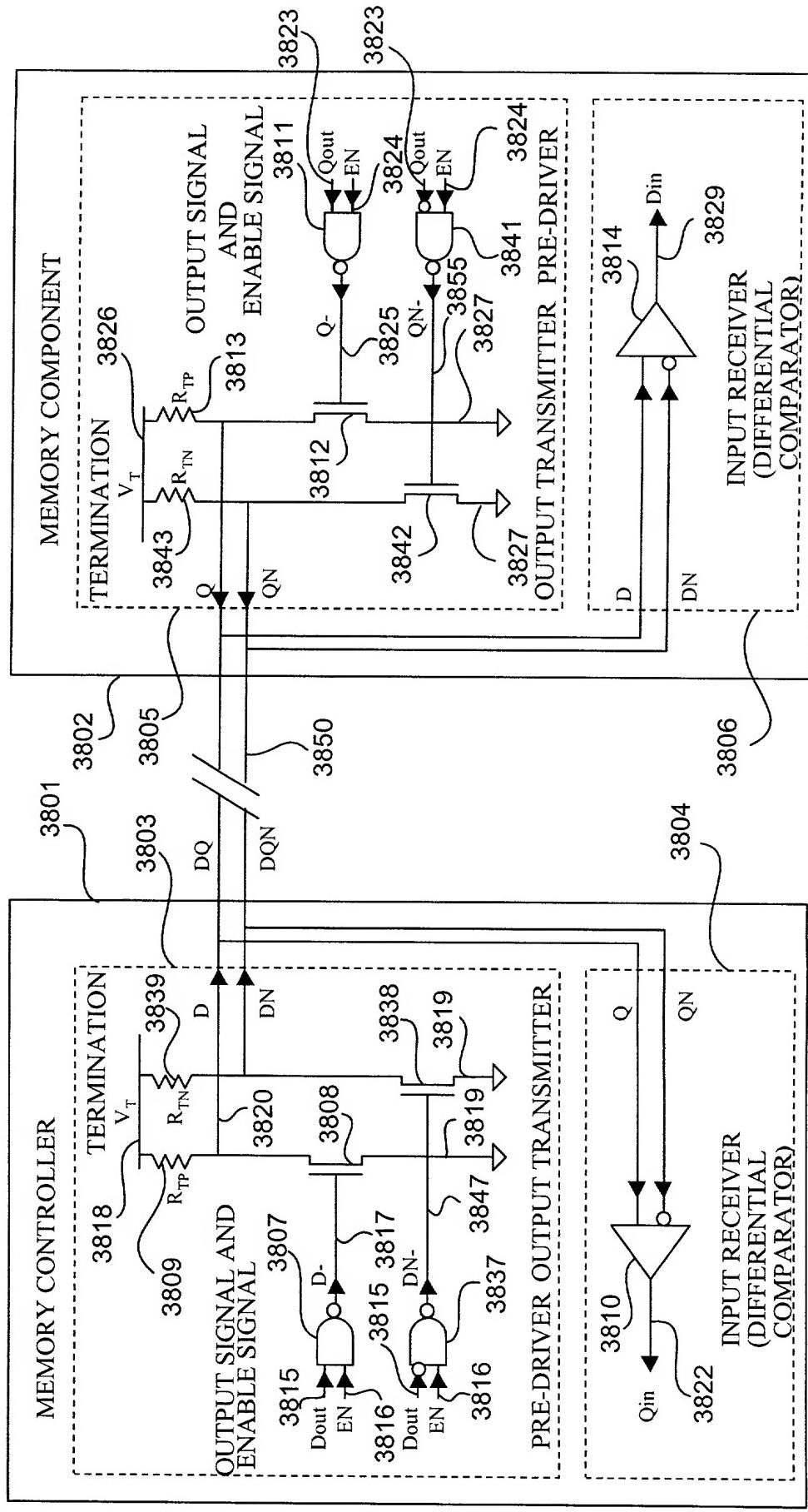


FIG. 37

FIG. 38



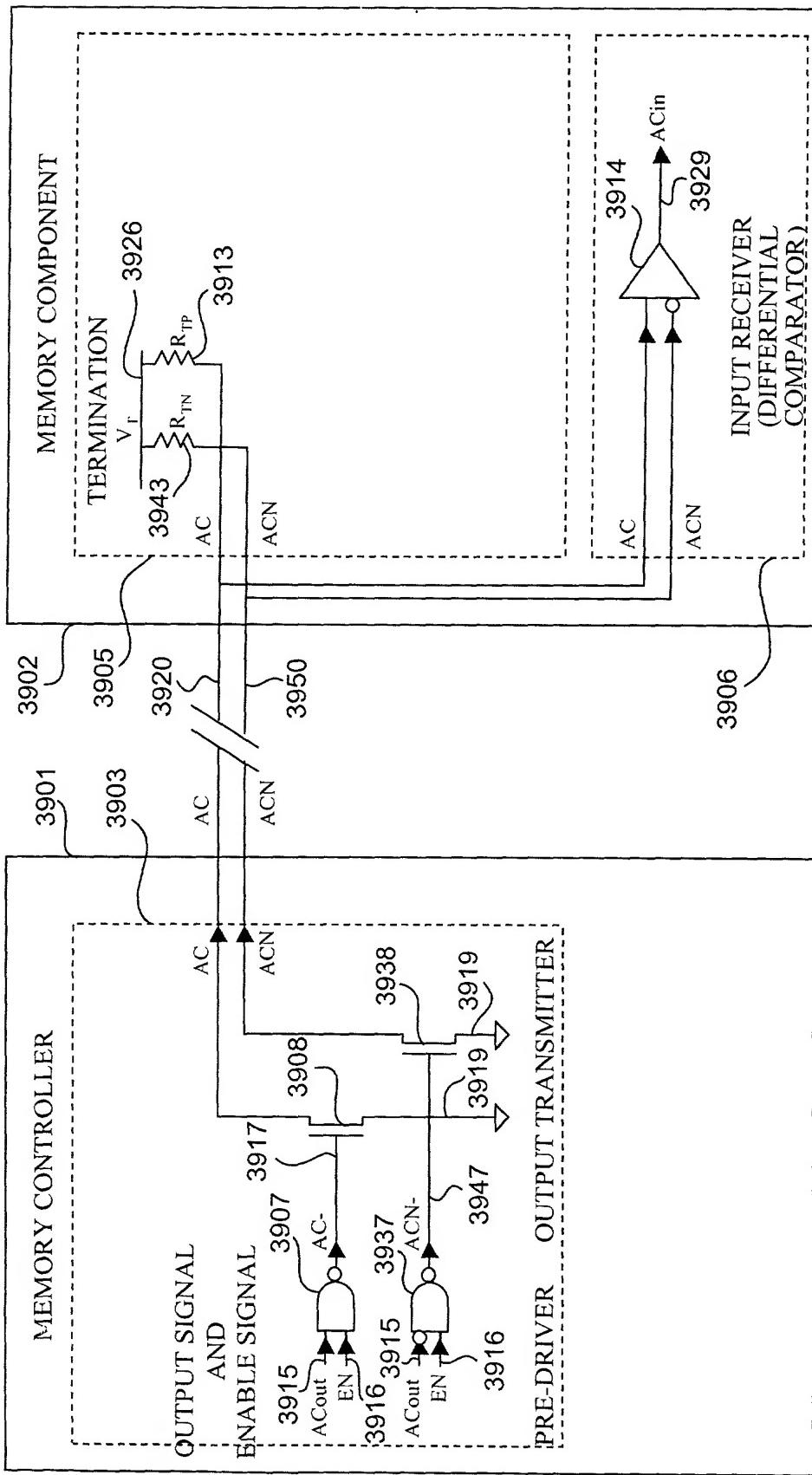


FIG. 39